SSD1803

Advance Information

100 x 34 STN
LCD Segment / Common Mono Driver with Controller

Appendix: IC Revision history of SSD1803 Specification

Version	Change Items	Effective Date
0.10	1st Release	04-Mar-09
0.20	Die mark: B3GA2 Revised Pads Coordinate on P.10, 11 (2um movement) Revised Pin description of EXT pin to "pull-low internally" on P.13	09-Jul-09
1.0	Die mark: B3GA2+ Revised Power Supply VDD and VCI range	06-Oct-09
2.0	P.65-66 Added Application Example for 2 line and 4-line mode	10-Feb-10

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1 GENERAL DESCRIPTION

SSD1803 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix character display system. It consists of 134 high voltage driving output pins for driving 100 Segments, 34 Commons. It can display 1, 2 or 4 lines with 5x8 or 6x8 dots format.

SSD1803 displays character directly from its internal 9,600 bits (240 characters x 5 x 8 dots) Character Generator ROM (CGROM). All the character codes are stored in the 640 bits (80 characters) Data Display RAM (DDRAM). User defined character can be loaded via 512 bits (8 characters) Character Generator RAM (CGRAM). In addition, there is a 128 bits Icon RAM for Icon display. Data/ Commands are sent from general MCU through software selectable 4/ 8-bit Parallel Interface or Serial Peripheral Interface.

SSD1803 embeds a DC-DC Converter and oscillator which reduce the number of external components. With the special design on minimizing power consumption and die size, SSD1803 is suitable for portable battery-driven applications requiring a long operation period and a compact size.

2 FEATURES

- Power supply: VCI = 2.4V ~ VDD
  VDD = 2.7V ~ 3.45V
- LCD driving output voltage (VLCD = V5-VSS): 3.0 to 10.0V (Internal power supply mode)
  3.0 to 13.0V (External power supply mode)
- Low current power down mode
- On Chip 2x/3x DC-DC Converter/External Power Supply
- Internal or External voltage divider
- Programmable bias ratio when internal divider is used: 1/4, 1/5, 1/6, 1/7
- Internal Oscillator with an external resistor
- Programming duty cycle: 1/17, 1/33
- 1, 2 or 4 lines with 5x8 or 6x8 dots format display
- 8/4-bit Parallel Interface and Serial Peripheral Interface
- Bi-direction shift function
- All character reverse display
- Display shift per line
- Automatic power on reset
- On-Chip Memories
  - Character Generator ROM (CGROM): 9600 bits (240 characters x 5 x 8 dot)
  - Character Generator RAM (CGRAM): 64 x 8 bits (8 characters)
  - Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
  - Segment Icon RAM (SEGRAM): 16 x 8 bits (96 icons max.)
- Available in Bare Die

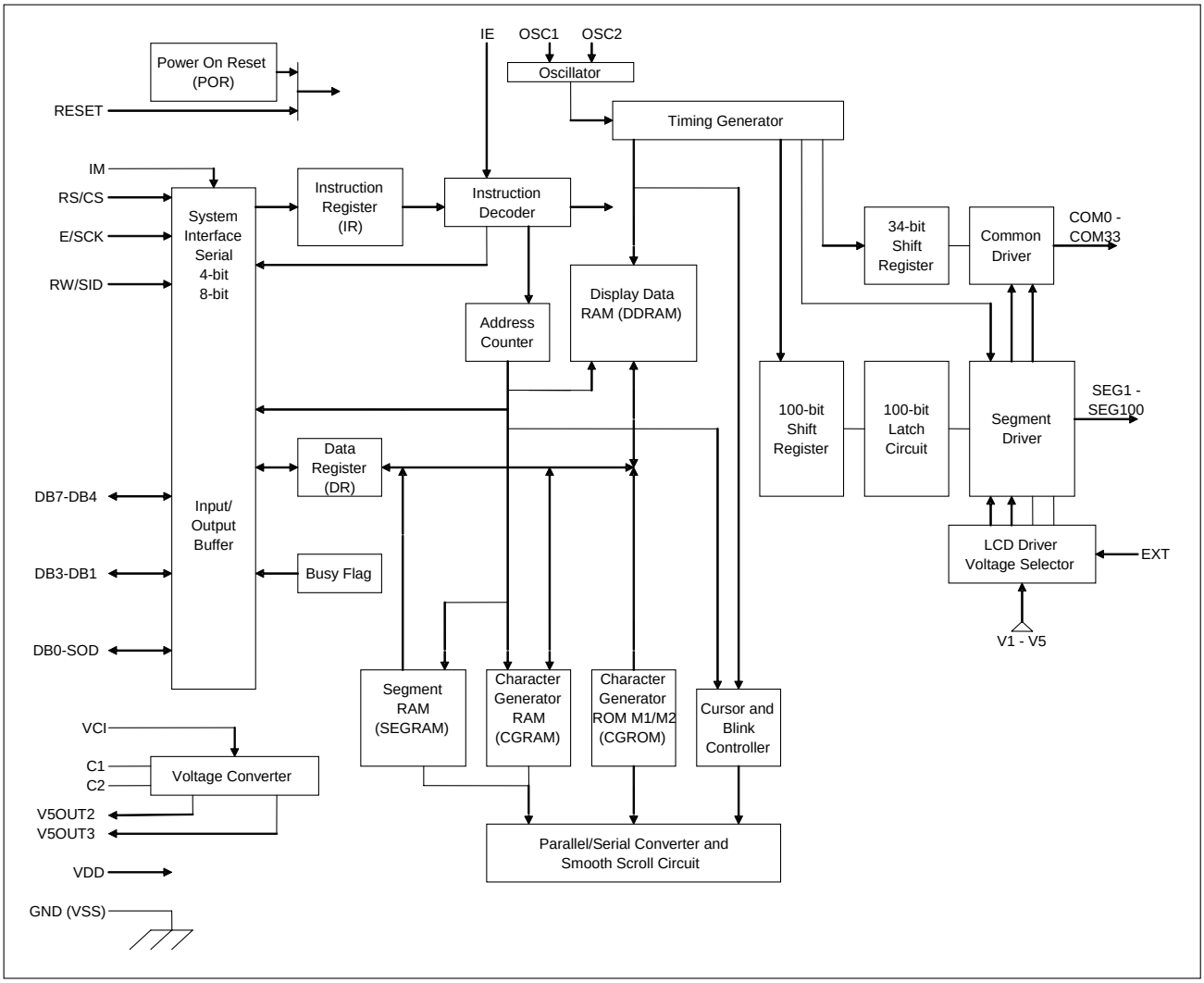
3 ORDERING INFORMATION

Table 3-1 Ordering Information

Ordering Part Number	Package Form	Reference on CGROM Character Code
SSD1803M1V	Bare Die	Appendix I
SSD1803M2V	Bare Die	Appendix II

4 BLOCK DIAGRAM

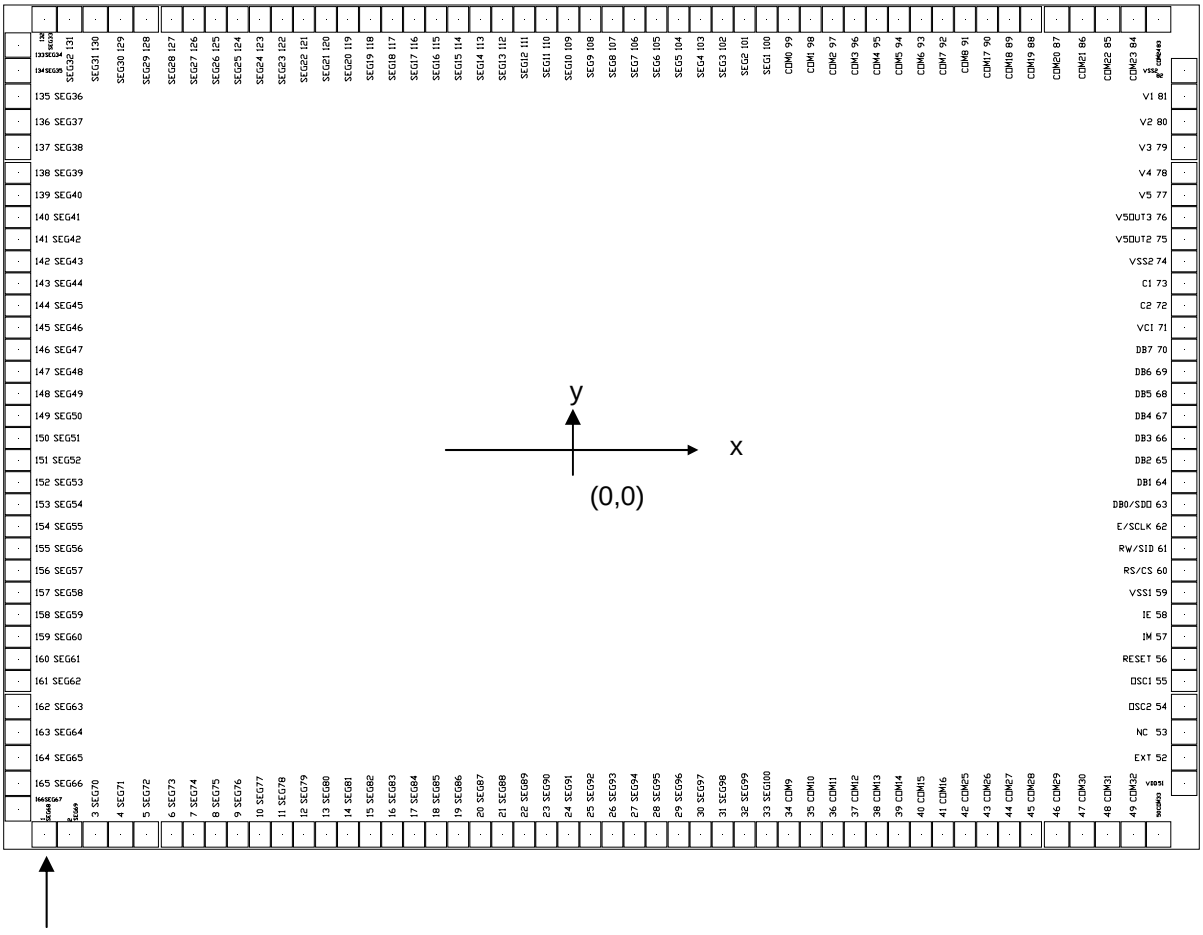
Figure 4-1 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 SSD1803 Die Pad Floor Plan (Die Face Up)

* Note: Die size is subject to change upon design completion*



Die Size (after sawing)	5184±50μm x 3731±50μm
Die Thickness	300±25μm

Table 5-1 SSD1803 Die Pad Coordinates (Pad center)

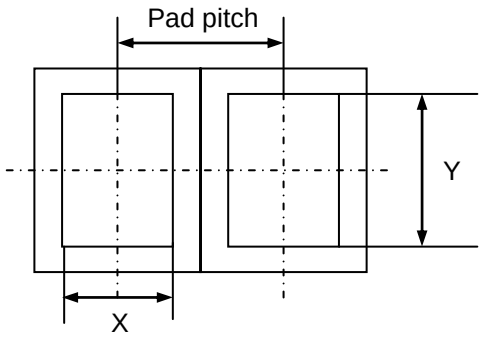
* Note: Pad Coordinates listed below is subjected to change upon design completion*

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	SEG68	-2401	-1750	51	VDD	2510	-1532	101	SEG2	619	1751
2	SEG69	-2291	-1750	52	EXT	2510	-1422	102	SEG3	524	1751
3	SEG70	-2181	-1750	53	NC	2510	-1312	103	SEG4	429	1751
4	SEG71	-2071	-1750	54	OSC2	2510	-1202	104	SEG5	334	1751
5	SEG72	-1961	-1750	55	OSC1	2510	-1092	105	SEG6	239	1751
6	SEG73	-1851	-1750	56	RESET	2510	-997	106	SEG7	144	1751
7	SEG74	-1756	-1750	57	IM	2510	-902	107	SEG8	49	1751
8	SEG75	-1661	-1750	58	IE	2510	-807	108	SEG9	-46	1751
9	SEG76	-1566	-1750	59	VSS1	2510	-712	109	SEG10	-141	1751
10	SEG77	-1471	-1750	60	RS/CS	2510	-617	110	SEG11	-236	1751
11	SEG78	-1376	-1750	61	RW/SID	2510	-522	111	SEG12	-331	1751
12	SEG79	-1281	-1750	62	E/SCLK	2510	-427	112	SEG13	-426	1751
13	SEG80	-1186	-1750	63	DB0/SDO	2510	-332	113	SEG14	-521	1751
14	SEG81	-1091	-1750	64	DB1	2510	-237	114	SEG15	-616	1751
15	SEG82	-996	-1750	65	DB2	2510	-142	115	SEG16	-711	1751
16	SEG83	-901	-1750	66	DB3	2510	-47	116	SEG17	-806	1751
17	SEG84	-806	-1750	67	DB4	2510	48	117	SEG18	-901	1751
18	SEG85	-711	-1750	68	DB5	2510	143	118	SEG19	-996	1751
19	SEG86	-616	-1750	69	DB6	2510	238	119	SEG20	-1091	1751
20	SEG87	-521	-1750	70	DB7	2510	333	120	SEG21	-1186	1751
21	SEG88	-426	-1750	71	VCI	2510	428	121	SEG22	-1281	1751
22	SEG89	-331	-1750	72	C2	2510	523	122	SEG23	-1376	1751
23	SEG90	-236	-1750	73	C1	2510	618	123	SEG24	-1471	1751
24	SEG91	-141	-1750	74	VSS2	2510	713	124	SEG25	-1566	1751
25	SEG92	-46	-1750	75	V5OUT2	2510	808	125	SEG26	-1661	1751
26	SEG93	49	-1750	76	V5OUT3	2510	903	126	SEG27	-1756	1751
27	SEG94	144	-1750	77	V5	2510	998	127	SEG28	-1851	1751
28	SEG95	239	-1750	78	V4	2510	1093	128	SEG29	-1961	1751
29	SEG96	334	-1750	79	V3	2510	1203	129	SEG30	-2071	1751
30	SEG97	429	-1750	80	V2	2510	1313	130	SEG31	-2181	1751
31	SEG98	524	-1750	81	V1	2510	1423	131	SEG32	-2291	1751
32	SEG99	619	-1750	82	VSS2	2510	1533	132	SEG33	-2401	1751
33	SEG100	714	-1750	83	COM24	2404	1751	133	SEG34	-2514	1643
34	COM9	809	-1750	84	COM23	2294	1751	134	SEG35	-2514	1533
35	COM10	904	-1750	85	COM22	2184	1751	135	SEG36	-2514	1423
36	COM11	999	-1750	86	COM21	2074	1751	136	SEG37	-2514	1313
37	COM12	1094	-1750	87	COM20	1964	1751	137	SEG38	-2514	1203
38	COM13	1189	-1750	88	COM19	1854	1751	138	SEG39	-2514	1093
39	COM14	1284	-1750	89	COM18	1759	1751	139	SEG40	-2514	998
40	COM15	1379	-1750	90	COM17	1664	1751	140	SEG41	-2514	903
41	COM16	1474	-1750	91	COM8	1569	1751	141	SEG42	-2514	808
42	COM25	1569	-1750	92	COM7	1474	1751	142	SEG43	-2514	713
43	COM26	1664	-1750	93	COM6	1379	1751	143	SEG44	-2514	618
44	COM27	1759	-1750	94	COM5	1284	1751	144	SEG45	-2514	523
45	COM28	1854	-1750	95	COM4	1189	1751	145	SEG46	-2514	428
46	COM29	1964	-1750	96	COM3	1094	1751	146	SEG47	-2514	333
47	COM30	2074	-1750	97	COM2	999	1751	147	SEG48	-2514	238
48	COM31	2184	-1750	98	COM1	904	1751	148	SEG49	-2514	143
49	COM32	2294	-1750	99	COM0	809	1751	149	SEG50	-2514	48
50	COM33	2404	-1750	100	SEG1	714	1751	150	SEG51	-2514	-47

Pad #	Signal	X-pos	Y-pos
151	SEG52	-2514	-142
152	SEG53	-2514	-237
153	SEG54	-2514	-332
154	SEG55	-2514	-427
155	SEG56	-2514	-522
156	SEG57	-2514	-617
157	SEG58	-2514	-712
158	SEG59	-2514	-807
159	SEG60	-2514	-902
160	SEG61	-2514	-997
161	SEG62	-2514	-1092
162	SEG63	-2514	-1202
163	SEG64	-2514	-1312
164	SEG65	-2514	-1422
165	SEG66	-2514	-1532
166	SEG67	-2514	-1642

Pad Size

Pad #	X [um]	Y[um]	Pad pitch [um] (Min)
1-5, 46-54, 79-87, 128-137, 162-166	105	110	110
6-45, 55-78, 88-127, 138-161	90	110	95



6 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
GND = System VSS

Table 6-1 : Power Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
VCI	P	Power Supply for Analog Circuits	-	Input voltage to the voltage converter to generate LCD drive voltage
VDD	P	Power Supply for Logic Blocks	-	Power supply for logic circuit (VDD should rise within 10ms)
VSS1	GND	Ground of Power Supply	-	System ground pin of the IC for digital part
VSS2	GND	Ground of Power Supply	-	System ground pin of the IC for analog part

Table 6-2 : LCD Driver Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
V1 –V5	IO	LCD Power Supply	Open	Bias voltage level for LCD driving
C1, C2	I	External Capacitor	-	Connect to external capacitor when voltage converter is used
V5OUT2	O	x2 Converter Output	Open	Output of the x2 voltage converter
V5OUT3	O	x3 Converter Output	Open	Output of the x3 voltage converter

Table 6-3 : System Control Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
OSC1	I	Oscillator	-	When internal oscillator is used, connect external Rf resistor between OSC1 and OSC2. If external clock is used, connect it to OSC1
OSC2	O			
IE	I	Instruction Set Select	-	When IE=”High”, instruction set 1 is selected. When IE = “Low”, instruction set 2 is used.
IM	I	Interface Mode Select	-	Select the interface mode. When IM=”High”: 4-bit/8-bit bus mode When IM=”Low”: serial mode
EXT	IO	External Voltage Divider Select (VDD or Open)	-	Select external or internal voltage divider This pin is pull-low internally EXT=”H”: select external voltage divider EXT=Open: select internal voltage divider

Table 6-4 : MCU Interface Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
RS/CS	I	Register Select / Chip Select	-	When in bus mode, used as register select. When RS/CS=”High”, data register is selected. When RS/CS=”Low”, instruction register is selected. When in serial mode, used as chip select. When RS/CS=”High”, not selected. When RS/CS =”Low”, selected.
RW/SID	I	Read/Write / Serial Input Data	-	When in bus mode, used as read/write select. When RW/SID=”high”, read operation. When RW/SID=”Low”, write operation. When in serial mode, used as serial data input pin.
E/SCLK	I	RW Enable / Serial Clock	-	When in bus mode, used as read/write enable signal. When in serial mode, used as serial clock input pin.
RESET	I	Reset Pin	-	System reset pin
DB0/SOD	IO	Data Bus 0 / Serial Output Data	-	When in 8-bit bus mode, used as lowest bi-direction data bit. During in 4-bit bus mode, open this pin. When in serial mode, used as serial data output pin. If not is read operation, open this pin.
DB1 - DB3	IO	Data Bus 1-7	-	When in 8-bit bus mode, used as low order bi-directional data bus. When in 4-bit bus mode or serial mode, open these pins.
DB4 – DB7	IO		-	When in 8-bot bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for busy flag output. During serial mode, open these pins.

Table 6-5 : LCD Driver Output Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
SEG1 - SEG100	O	Segment Output	Open	Segment signal output for LCD drive
COM0 - COM33	O	Common Output	Open	Common signal output for LCD drive

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Programmable Duty Cycles

5-dot Font Width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable Characters	Possible Icons
1	1/17	1 line of 40 characters	80
2	1/33	2 lines of 40 characters	80
4	1/33	4 line of 20 characters	80

6-dot Font Width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable Characters	Possible Icons
1	1/17	1 line of 32 characters	96
2	1/33	2 lines of 32 characters	96
4	1/33	4 line of 16 characters	96

7.2 System Interface

This chip has all three kinds interface type with MPU: serial, 4-bit bus and 8-bit bus. Serial and bus (4-bit/8-bit) is selected by IM input, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically. The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS/CS input pin in 4-bit/8-bit bus mode (IM = "High") or RS bit in serial mode (IM = "Low").

RS	R/W	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)/ Part ID

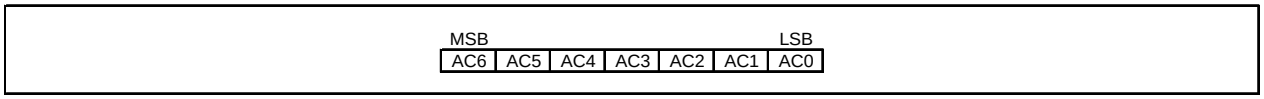
7.3 Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7. Before executing the next instruction, be sure that BF is not high.

7.4 Display Data Ram (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 7-1.)

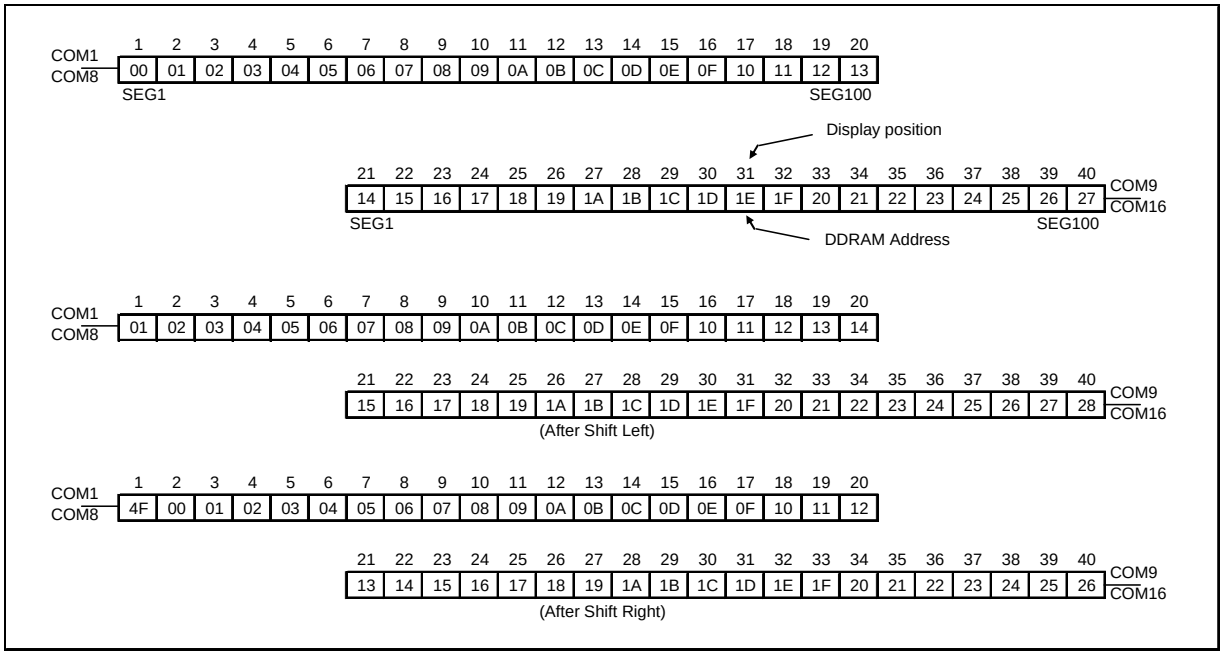
Figure 7-1 DDRAM Address



Display of 5-Dot Font Width Character
5-dot 1-line Display

In case of 1-line display with 5-dot font, the address range of DDRAM is 00H-4FH. (refer to Figure 7-2)

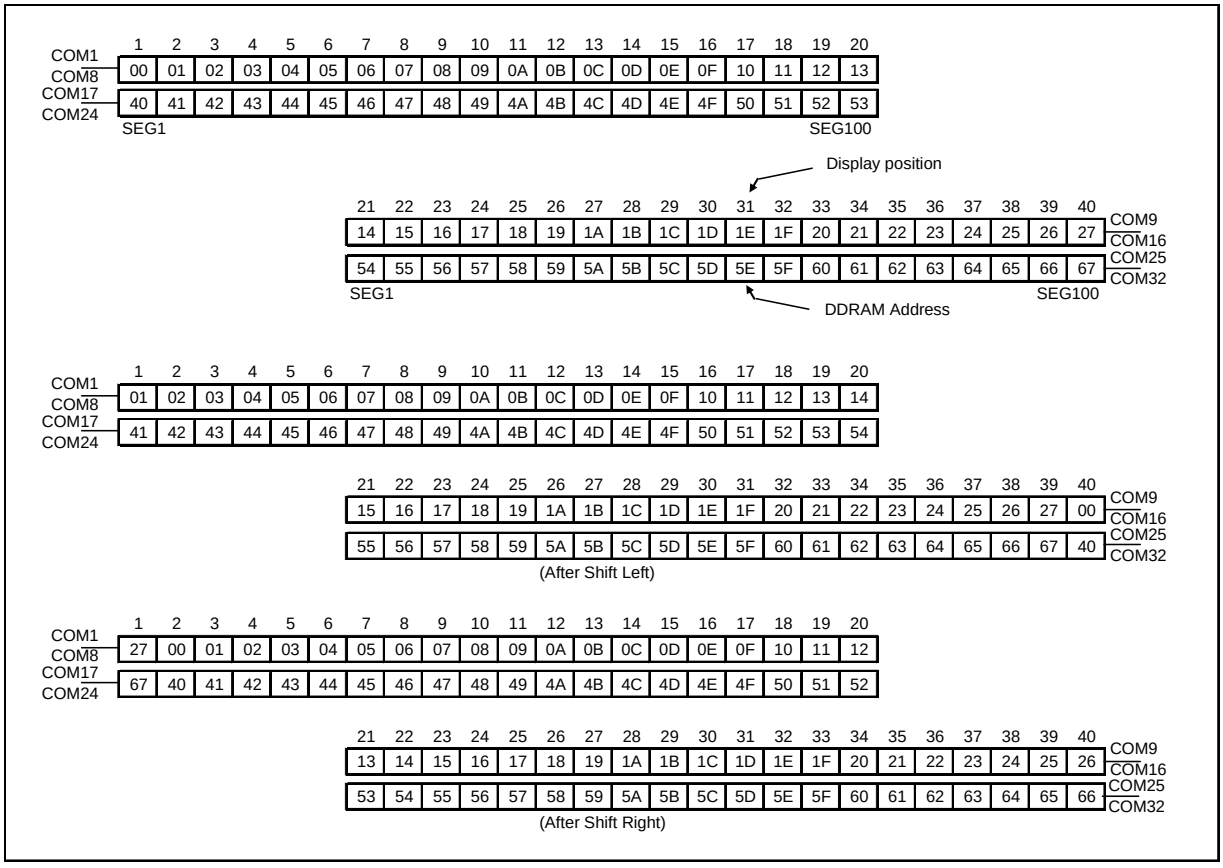
Figure 7-2 1-line x 40ch. Display (5-dot Font Width)



5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-3).

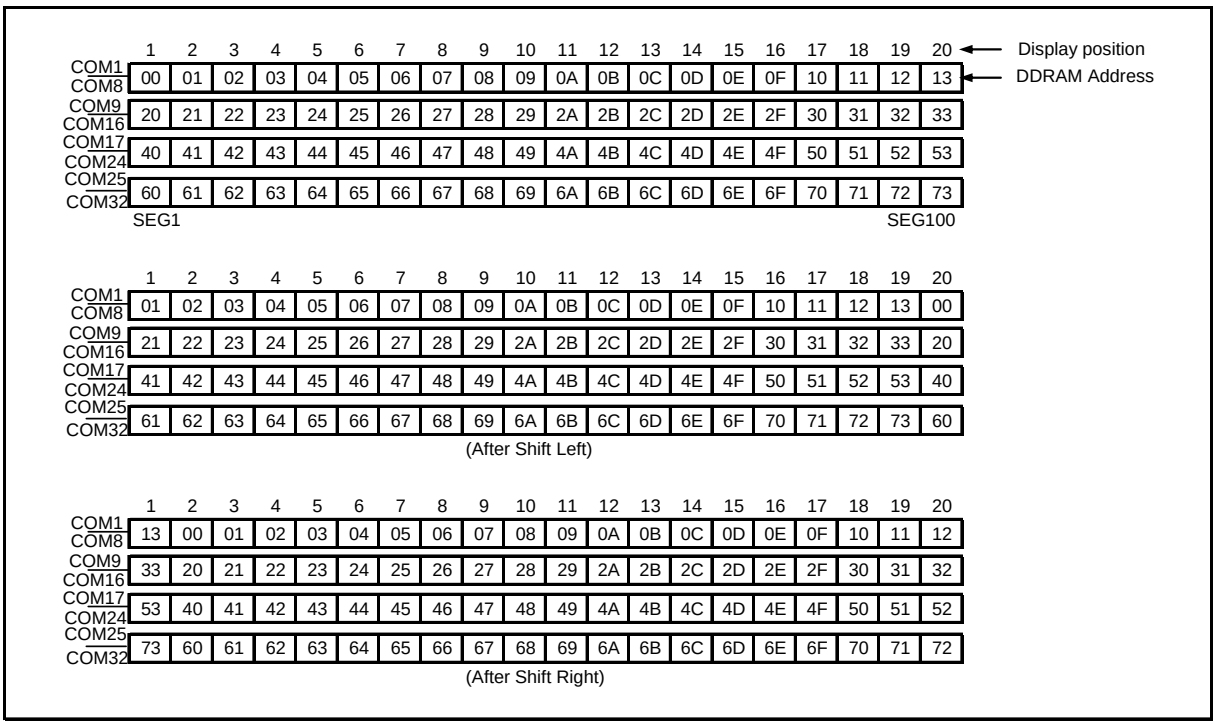
Figure 7-3 2-line x 40ch. Display (5-dot Font Width)



5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-4).

Figure 7-4 4-line x 20ch. Display (5-dot Font Width)



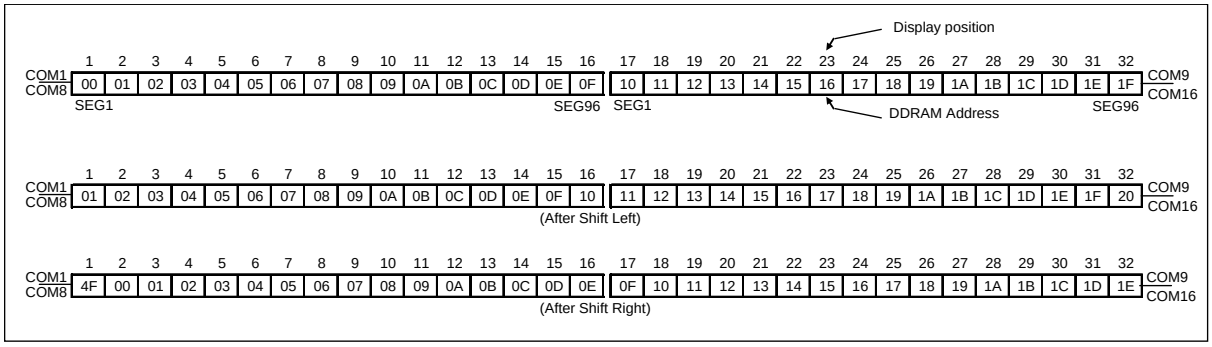
DISPLAY OF 6-DOT FONT WIDTH CHARACTER

When this device is used in 6-dot font width mode, SEG97, SEG98, SEG99 and SEG100 must be opened.

6-dot 1-line Display

In case of 1-line display with 6-dot font, the address range of DDRAM is 00H-4FH (refer to Figure 7-5).

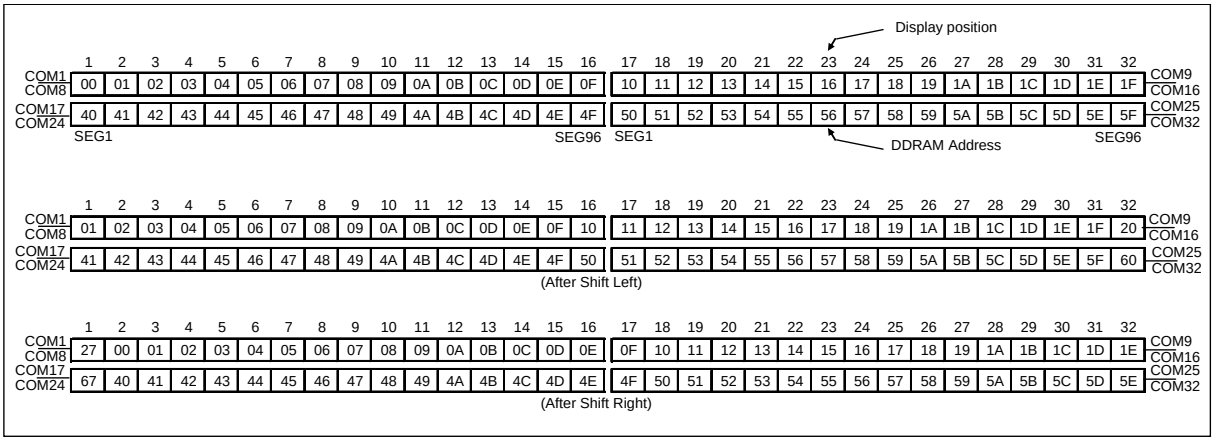
Figure 7-5 1-line x 32ch. Display (6-dot Font Width)



6-dot 2-line Display

In case of 2-line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-6).

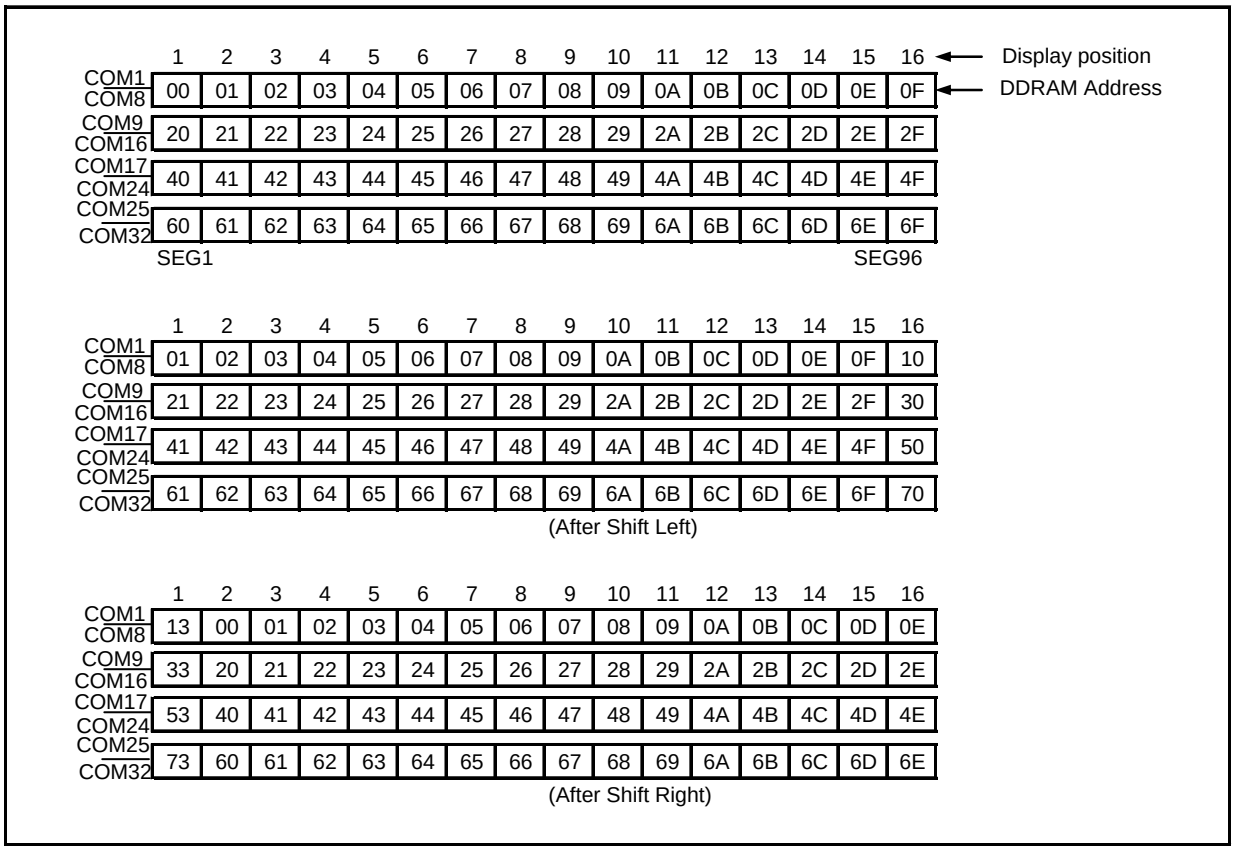
Figure 7-6 2-line x 32ch. Display (6-dot Font Width)



6-dot 4-line Display

In case of 4-line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-7).

Figure 7-7 4-line x 16ch. Display (6-dot Font Width)



7.5 Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

7.6 Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0-DB6.

7.7 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

7.8 LCD Driver Circuit

LCD Driver circuit has 34 common and 100 segment signals for LCD driving. Data from SEGRAM/CGRAM/CGROM is transferred to 100-bit segment latch serially, and then it is stored to 100-bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 100-bit segment latch. In case of 1-line display mode, COM0-COM17 have 1/17 duty, and in 2-line or 4-line mode, COM0-COM33 have 1/33 duty ratio.

7.9 CGROM (Character Generator ROM)

CGROM has 5 x 8 dots 240 Character Pattern.

7.10 CGRAM (Character Generator RAM)

CGRAM has up to 5 x 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 7-1).

Table 7-1 Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

5x8 dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	Number
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern1
											0	0	1				1	0	0	0	1	
				.							0	1	0				1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0		.		1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern8
											0	0	1				1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

6 x 8 Dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	Number
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern1
											0	0	1			0	1	0	0	0	1	
				.							0	1	0			0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0		.	0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	Pattern8
											0	0	1			0	1	0	0	0	1	
				.					.		0	1	0		.	0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0			0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	

1. When BE (Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
   In case of 5-dot font width, when B1 = "1", enabled dots of P0-P4 will blink, and when B1 = "0" and B0 = "1", enabled dots in P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.
   In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.
2. "X": Don't care

7.11 SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During 1-line display mode, COM0 (COM17) makes the data of SEGRAM enable to display icons. When used in 2/4-line display mode COM0 (COM33) does that. Its higher 2-bit are blinking control data, and lower 6-bits are pattern data (refer to Table 7-2 and Figure 7-8).

Table 7-2 Relationship between SEGRAM Address and Display Pattern

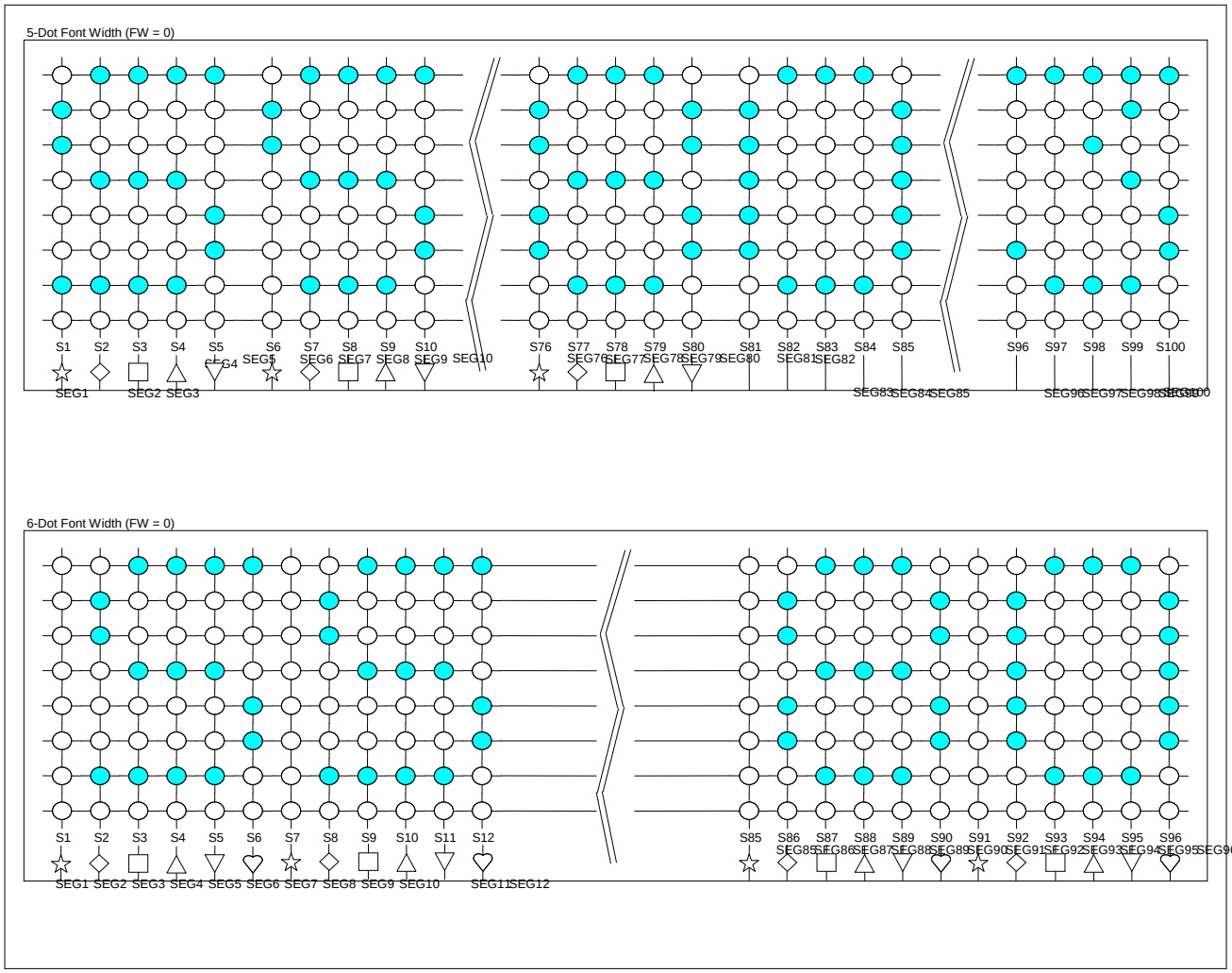
SEGRAM Address				SEGRAM Data Display Pattern															
				5-dot Font Width								6-dot Font Width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	X	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	X	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	X	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	X	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	X	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	X	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	X	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	X	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	X	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	X	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	X	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	X	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	X	S61	S62	S62	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	X	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	X	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	X	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96

1. B1, B0: Blinking control bit

Control Bit	Blinking Port	
BE B1 B0	5-dot font width	6-dot font width
0 X X	No blink	No blink
1 0 0	No blink	No blink
1 0 1	D4	D5
1 1 X	D4 - D0	D5 - D0

1. S1-S80 : Icon pattern ON/OFF in 5-dot font width
   S1-S96 : Icon pattern ON/OFF in 6-dot font width
2. "X": Don't care.

Figure 7-8 Relationship between SEGRAM and Segment Display



7.12 Interface with MPU

SSD1803 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. So you can use any type 4 or 8-bit MPU.
In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

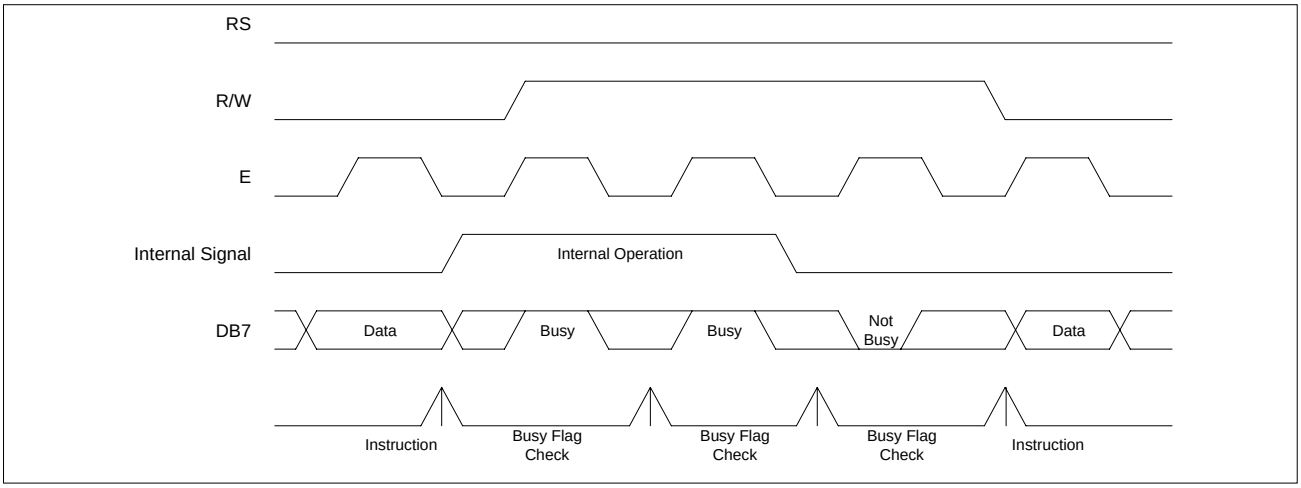
- When interfacing data length is 4-bit, only 4 ports, from DB4 - DB7, are used as data bus.
- At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy flag outputs "High" after the second transfer are ended.
- When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 -DB7.
- If IM is set to "Low", serial transfer mode is set.

INTERFACE WITH MPU IN BUS MODE

Interface with 8-bit MPU

If 8-bit MPU is used, SSD1803 can connect directly with that. In this case, port E, RS, R/W and DB0 - DB7 need to interface each other. Example of timing sequence is shown below.

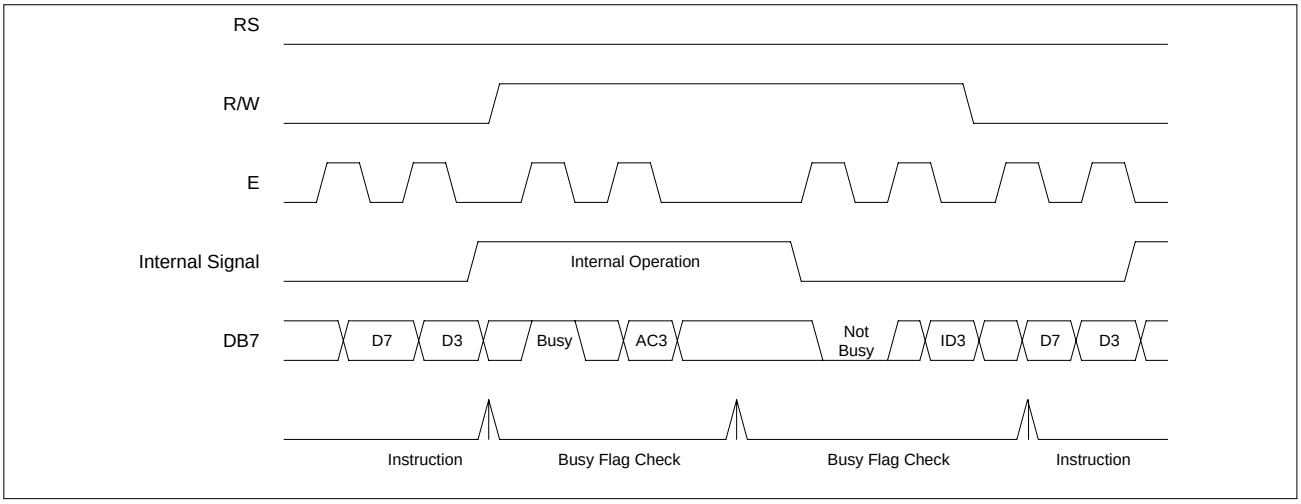
Figure 7-9 Example of 8-bit Bus Mode Timing Sequence



Interface with 4-bit MPU

If 4-bit MPU is used, SSD1803 can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

Figure 7-10 Example of 4-bit Bus Mode Timing Sequence



INTERFACE WITH MPU IN SERIAL MODE

When IM port input is "Low", serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If you want to use SSD1803 with other chips, chip select port (CS) can be used. By setting CS to "Low", SSD1803 can receive SCLK input. If CS is set to "High", SSD1803 reset the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding 5 "High" bits, read write control bit (R/W), register selection bit (RS) and end bit that indicates the end of start byte. Whenever succeeding 5 "High" bits are detected by SSD1803, it makes serial transfer counter reset and ready to receive next information.

The next input data are register selection bit that determine which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to Figure 7-11 and Figure 7-12)

Write Operation (R/W = 0)

After start byte is transferred from MPU to SSD1803, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer. To transfer several bytes continuously without changing RS bit and RW bit, start byte transfer is needed only at first starting time. Namely, after first start byte is transferred, real data can be transferred succeeding.

Read Operation (R/W = 1)

After start byte is transferred to SSD1803, MPU can receive 8-bit data through the SOD port at a time from the LSB. Wait time is needed to insert between start byte and data reading, because internal reading from RAM requires some delay. Continuous data reading is possible like serial write operation. It also needs only one start byte, only if you insert some delay between reading operations of each byte. During the reading operation, SSD1803 observes succeeding 5 "High" from MPU. If it is detected, SSD1803 restarts serial operation at once and ready to receive RS bit. So in continuous reading operation, SID port must be "Low".

Figure 7-11 Timing Diagram of Serial Data Transfer

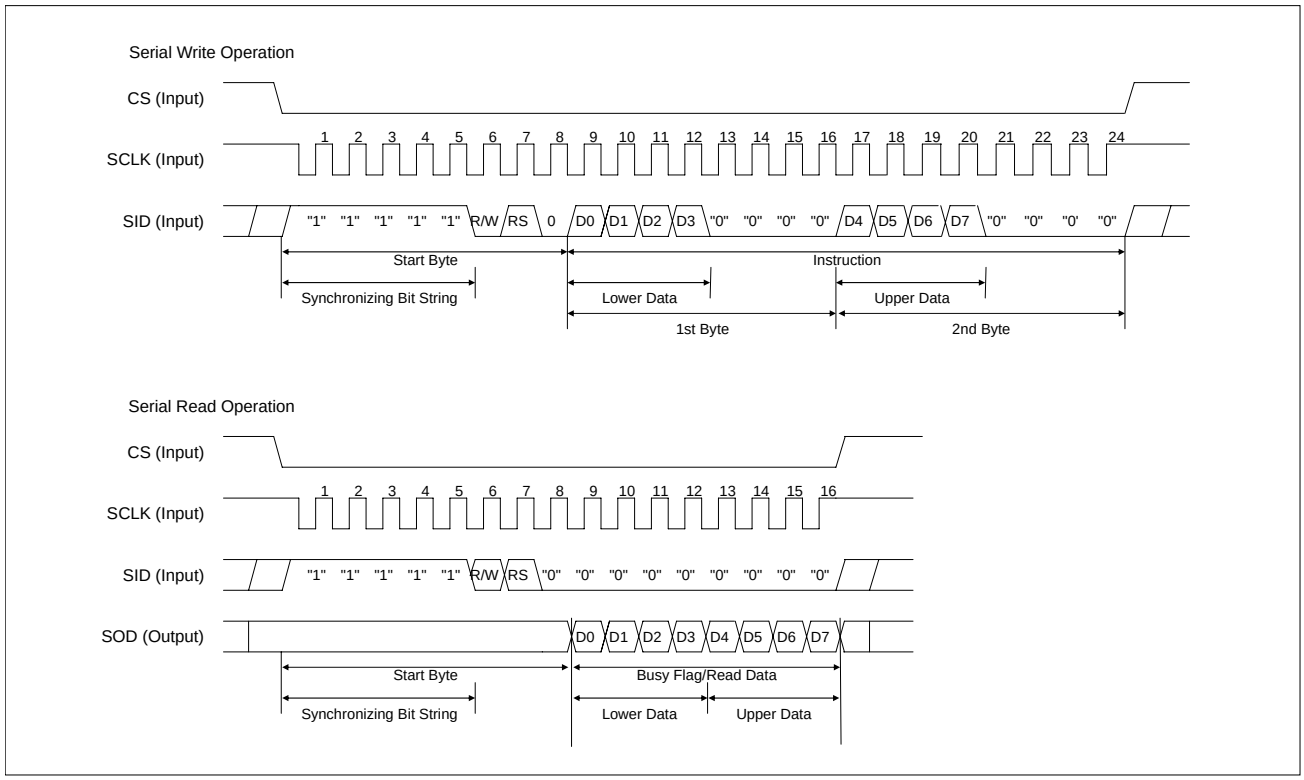
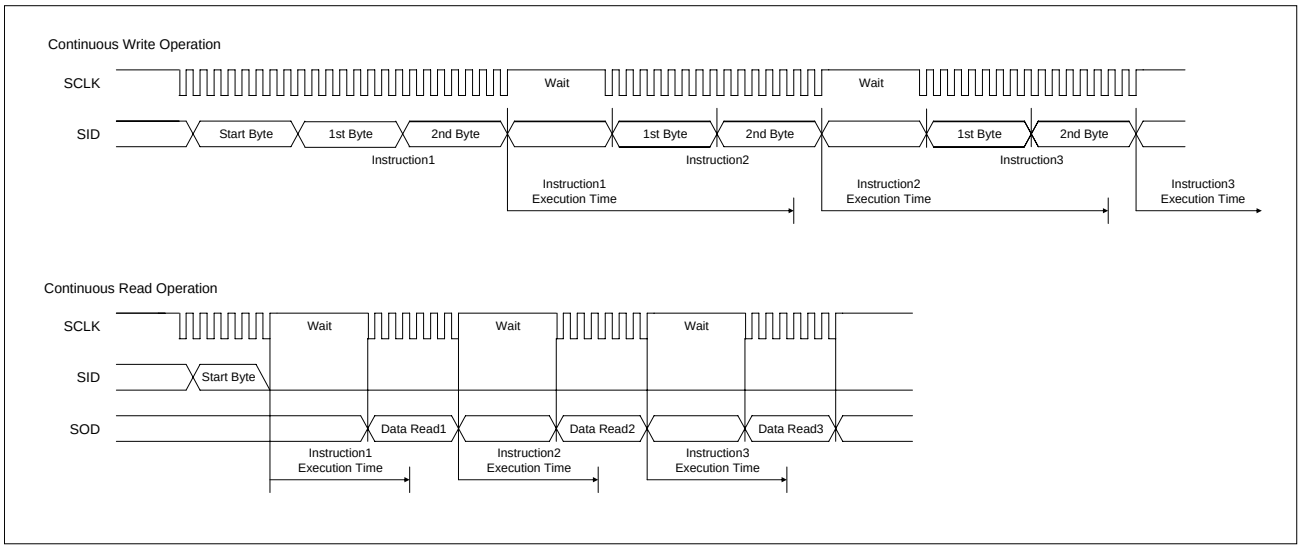


Figure 7-12 Timing Diagram of Continuous Data Transfer



8 COMMAND TABLE

To overcome the speed difference between internal clock of SSD1803 and MPU clock, SSD1803 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 8-1 and Table 8-2) Instruction can be divided largely four kinds,

- SSD1803 function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others.

The address of internal RAM is automatically increased or decreased by 1.

When IE = "High", SSD1803 is operated according to instruction set 1 (Table 8-1) and when IE = "Low", SSD1803 is operated according to instruction set 2 (Table 8-2).

NOTE**:** During internal operation, busy flag (DB7) is read high. Busy flag check must precede the next instruction. When an MPU program with Busy Flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

Table 8-1 Instruction Set 1 (IE = ”HIGH”)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.53ms
Return home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power down mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = "1": power down mode set, PD = "0": power down mode disable	39us
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1": increment, I/D = "0": decrement. S = "1": make display shift of the enabled lines by the DS4 DS1 bits in the shift enable instruction. S = "0": display shift disable	39us
	1	0	0	0	0	0	0	0	1	1	B/D	Segment bi-direction function. BID = "0": Seg1 -> Seg100, BID = "1": Seg100 -> Seg1.	
Display On/Off control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1": display on, D = "0": display off, C = "1": cursor on, C = "0": cursor off, B = "1": blink on, B = "0": blink off.	39us
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width, B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable NW = "1": 4-line display mode, NW = "0": 1-line or 2-line display mode	39us
Cursor or display shift / Bias ratio select	0	0	0	0	0	0	1	S/C	R/L	BS1	BS0	Cursor or display shift. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left. BS1:BS0 = “00”: 1/4 bias (POR at display line=1) BS1:BS0 = “01”: 1/5 bias BS1:BS0 = “10”: 1/6 bias (POR at display line=2 or 4) BS1:BS0 = “11”: 1/7 bias *Note: BS1 and BS0 are only activated in internal divider option	39us
Shift enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH = "1") Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.	39us

Scroll enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH = "0") Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.	39us
Function set	0	0	0	0	0	1	DL	N	RE (0)	DH	REV	Set interface data length DL = "1": 8-bit, DL = "0": 4-bit Numbers of display line when NW = "0", N = "1": 2-line, N = "0": 1-line Extension register, RE("0") Shift/scroll enable DH = "1": display shift enable DH = "0": dot scroll enable. Reverse bit REV = "1": reverse display, REV = "0": normal display.	39us
	1	0	0	0	0	1	DL	N	RE (1)	BE	0	Set DL, N, RE("1") CGRAM/SEGRAM blink enable BE = " 1/0": CGRAM/SEGRAM blink enable/disable	
set CGRAM address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39us
set SEGRAM address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39us
set DDRAM address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39us
set scroll quantity	1	0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.	39us
Read busy flag and address/ part ID	X	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. * In the Serial Interface, data can only be read in Continuous Read Operation, details please refer to Fig.7-12. BF = "1": busy state BF = "0": ready state	0us
write data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).	43us
read data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).	43us

NOTES**:**

1. When an MPU program with busy flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the "E" signal after the busy flag (DB7) goes to "Low"
2. "X": Don't care

Table 8-2 Instruction Set 2 (IE = ”Low”)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return home	X	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode set	X	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1": increment, I/D = "0": decrement. S = "1": make entire display shift of all lines during DDRAM write. S = "0": display shift disable	39us
Display On/Off control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1": display on, D = "0": display off, C = "1": cursor on, C = "0": cursor off, B = "1": blink on, B = "0": blink off.	39us
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width, B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable NW = "1": 4-line display mode, NW = "0": 1-line or 2-line display mode	39us
Cursor or display shift / Bias ratio select	0	0	0	0	0	0	1	S/C	R/L	BS1	BS0	Cursor or display shift. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left. BS1:BS0 = “00”: 1/4 bias (POR at display line=1) BS1:BS0 = “01”: 1/5 bias BS1:BS0 = “10”: 1/6 bias (POR at display line=2 or 4) BS1:BS0 = “11”: 1/7 bias *Note: BS1 and BS0 are only activated in internal divider option	39us
Scroll enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.	39us

Function set	0	0	0	0	0	1	DL	N	RE (0)	X	X	Set interface data length DL = "1": 8-bit DL = "0": 4-bit, numbers of display line when NW = "0", N = "1": 2-line N = "0": 1-line extension register, RE("0")	39us
	1	0	0	0	0	1	DL	N	RE (1)	BE	0	Set DL, N, RE("1") and CGRAM/SEGRAM blink enable (BE) BE = " 1/0": CGRAM/SEGRAM blink enable/disable	
set CGRAM address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39us
set SEGRAM address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39us
set DDRAM address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39us
set scroll quantity	1	0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.	39us
Read busy flag and address/ part ID	X	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. * In the Serial Interface, data can only be read in Continuous Read Operation, details please refer to Fig.7-12. BF = "1": busy state BF = "0": ready state	0us
write data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).	43us
read data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).	43us

Note:

1. When an MPU program with Busy Flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.
2. "X": Don’t care.

9 COMMAND DESCRIPTIONS

9.1 Command Set 1 (IE = “HIGH”)

9.1.1 Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

9.1.2 Return Home (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

9.1.3 Power Down Mode set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction. When PD = "High", it makes SSD1803 suppress current consumption except the current needed for data storage by executing next three functions.

- Make the output value of all the COM/SEG ports VSS
- Disable voltage converter to remove the current through the divide resistor of power supply. You can use this instruction as power sleep mode.
- When PD = "Low", power down mode becomes disabled.

9.1.4 Entry Mode Set

RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

- CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the shift enable instruction is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display like this function is not performed.

RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.

BID: Data shift direction of segment
When BID = "Low", segment data shift direction is set to normal order from SEG1 to SEG100.
When BID = "High", segment data shift direction is set to reverse from SEG100 to SEG1.
By using this instruction, you can raise the efficiency of application board area.

- The BID setting instruction is recommended to be set at the same time level of function set instruction.
- DB1 bit must be set to "1".

9.1.5 Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

9.1.6 Extended Function Set (RE = 1)

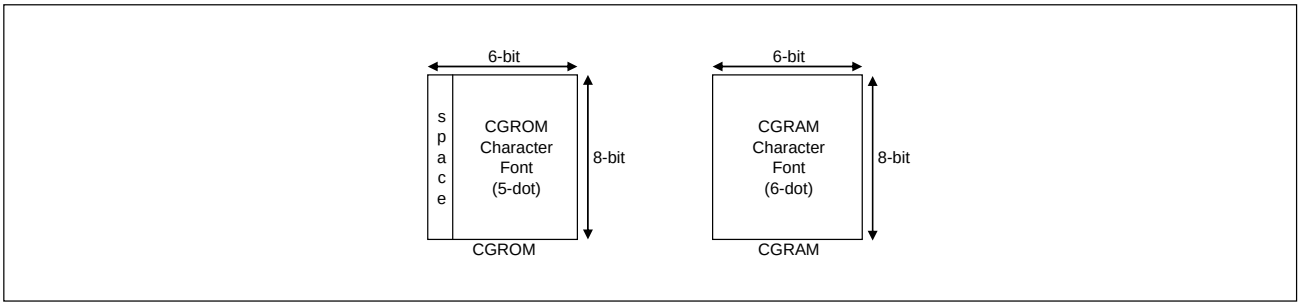
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW: Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(refer to Figure 9-1)
When FW = "Low", 5-dot font width is set.

B/W: Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

Figure 9-1 6-dot Font Width CGROM/CGRAM



9.1.7 Cursor or Display Shift / Bias Ratio Select (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	BS1	BS0

Shift right/left cursor position or display, without writing or reading of display data, this instruction is use to corrector search display data (refer to Table 9-1). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line enabled by DS1-DS4 in the shift enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed. During low power consumption mode, display shift may not be performed normally.

Table 9-1 Shift patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1.
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display.
1	1	Shift all the display to the right, cursor moves according to the display.

BS1, BS0: When internal voltage divider is used (EXT =Open), set the Bias Ratio according to following table:

BS1:BS0	Bias Ratio
00	1/4
01	1/5
10	1/6
11	1/7

9.1.8 Shift/Scroll Enable (RE = 1)

DH = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal scroll per line enable
This instruction makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If you want to scroll the line in 1-line display mode or the 1st line in 2-line display mode, set HS1 and HS2 to "High".
If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High". (refer to Table 9-2)

DH = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display shift per line enable this instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.
If you set DS1 and DS2 to "High" (enable) in 2 line mode, only the 1st line is shifted and the 2nd line is not shifted. When only DS1 = "High", only the half of the 1st line is shifted. If all the DS bits (DS1 to DS4) are set to "Low" (disable), no display is shifted.

Table 9-2 Relationship between DS and COM signal

Enable Bit	Enabled Common Signals During Shift	Description
HS1/DS1	COM1 - COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9 - COM16	
HS3/DS3	COM17 - COM24	
HS4/DS4	COM25 – COM32	

9.1.9 Function Set

RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(0)	DH	REV

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE: Extended function registers enable bit
At this instruction, RE must be "Low".

DH: Display shift enable selection bit.
When DH = "High", display shift per line becomes enable.
When DH = "Low", smooth dot scroll becomes enable.
This bit can be accessed only when IE pin input is "High".

REV: Reverse enable bit
When REV = "High", all the display data are reversed. Namely, all the white dots become black and black dots become white.
When REV = "Low", the display mode set normal display.

RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(1)	BE	0

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU.
So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE: Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, BID bit, HS/DS bits of shift/scroll enable instruction and BE bits of function set register can be accessed.

BE: CGRAM/SEGRAM data blink enable bit
If BE is "High", It makes user font of CGRAM and segment of SEGRAM blink. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

9.1.10 Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

9.1.11 Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	X	X	AC3	AC2	AC1	AC0

Set SEGRAM address to AC. This instruction makes SEGRAM data available from MPU.

9.1.12 Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H". In 4-line display mode (NW = 1), DDRAM address is from "00H" - "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" - "53H" in the 3rd line and from "60H" - "73H" in the 4th line.

9.1.13 Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units (Refer to Table 9-3). In this case SSD1803 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Table 9-3 Scroll Quantity According to HDS Bits

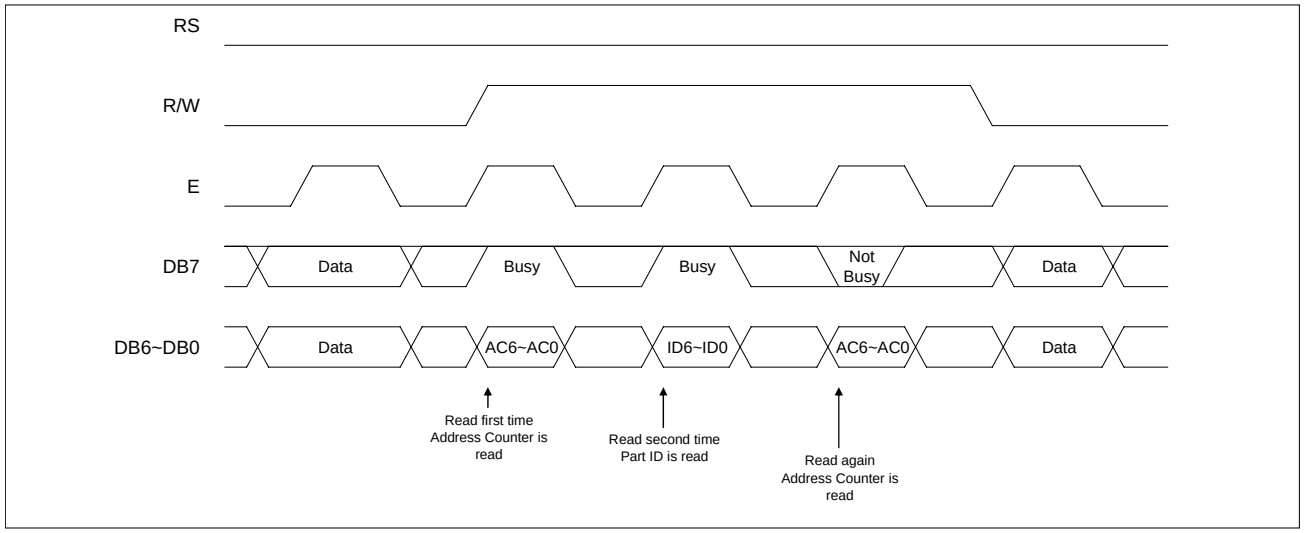
SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
0	0	0	0	1	1	Shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	Shift left by 47-dot
1	1	X	X	X	X	Shift left by 48-dot

9.1.14 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6/ID6	AC5/ID5	AC4/ID4	AC3/ID3	AC2/ID2	AC1/ID1	AC0/ID0

This instruction shows whether SSD1803 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter or the part ID. When the first time the instruction is run, you can read the address counter. When the instruction is run the second time, you can read the part ID (refer to Figure 9-2).

Figure 9-2 Read Busy Flag & Address/Part ID



Part Number	Part ID
SSD1803M1V	1111111
SSD1803M2V	1111110

9.1.15 Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM. The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAN address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

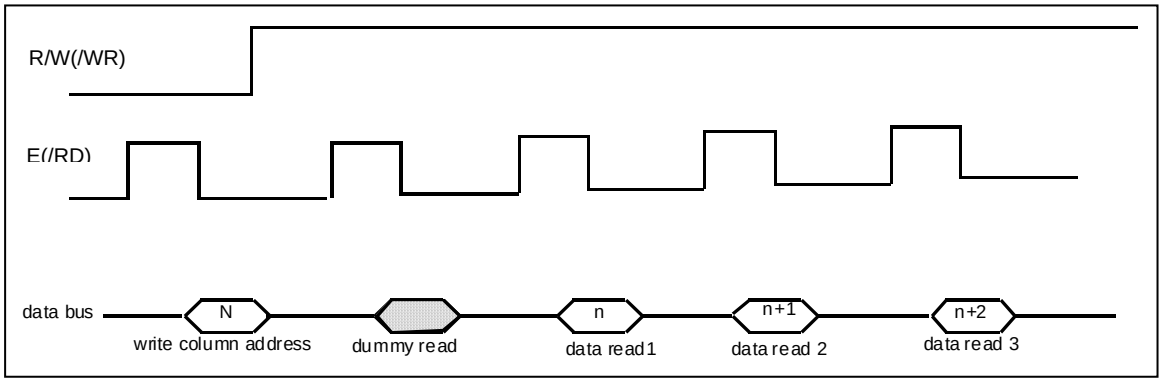
9.1.16 Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly. In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 9-3.

Figure 9-3: Display Data Read with the insertion of dummy read



*Remark: “n” - current DDRAM address contain, “n+1” - DDRAM address+1 contain

9.2 Command Set 2 (IE = “LOW”)

9.2.1 Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. And entry mode is set to increment mode (I/D = "1").

9.2.2 Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

9.2.3 Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D: Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

- CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the entire display of all lines is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, CGRAM/SEGRAM read/write operation, shift of entire display is not performed.

9.2.4 Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

9.2.5 Extended Function Set (RE = 1)

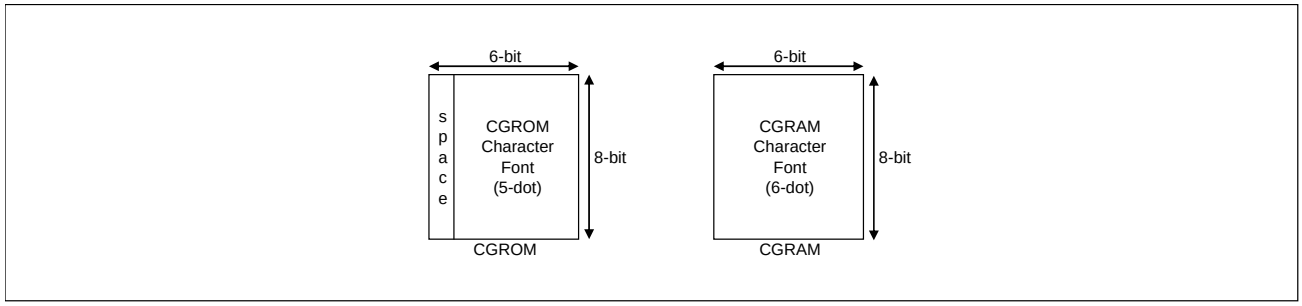
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW: Font width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0, including the leftmost pace bit of CGRAM.(Refer to Figure 9-4)
When FW = "Low", 5-dot font width is set.

B/W: Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction become don't care condition.

Figure 9-4 6-dot Font Width CGROM/CGRAM



9.2.6 Cursor or Display Shift / Bias Ratio Select (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	BS1	BS0

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data.(Refer to Table 9-4) during 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 9-4 Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1.
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display.
1	1	Shift all the display to the right, cursor moves according to the display.

BS1, BS0: When internal voltage divider is used (EXT = Open), set the Bias Ratio according to following table:

BS1:BS0	Bias Ratio
00	1/4
01	1/5
10	1/6
11	1/7

9.2.7 Scroll Enable (RE =1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal scroll per line enable
This instruction makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If you want to scroll the line in 1-line display mode or the 1st line in 2-line display mode, set HS1 and HS2 to "High". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High". (refer to Table 9-3)

9.2.8 Function Set

RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(0)	X	X

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE: Extended function registers enable bit
At this instruction, RE must be "Low".

RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(1)	BE	0

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 8-bit data by bus cycle.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE: Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, HS bits of scroll enable instruction and BE bits of function set register can be accessed.

BE: CGRAM/SEGRAM data blink enable bit
If BE is "High", It makes user font of CGRAM and segment of SEGRAM blink. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

9.2.9 Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

9.2.10 Set SEGRAM Address (RE =1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	X	X	AC3	AC2	AC1	AC0

Set SEGRAM address to AC. This instruction makes SEGRAM data available from MPU.

9.2.11 Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H". In 4-line display mode (NW = 1), DDRAM address is from "00H" to "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" to "53H" in the 3rd line and from "60H" to "73H" in the 4th line.

9.2.12 Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units (refer to Table 9-5). In this case SSD1803 execute dot smooth scroll from 1 to 48 dots.

Table 9-5 Scroll Quantity According to HDS Bits

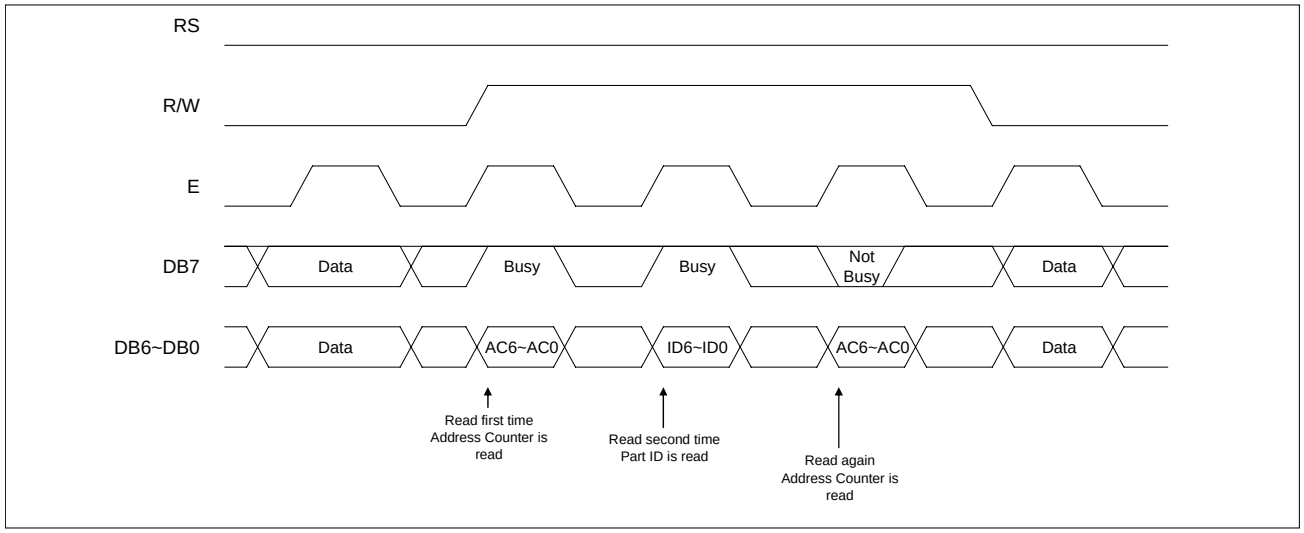
SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
0	0	0	0	1	1	Shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	Shift left by 47-dot
1	1	X	X	X	X	Shift left by 48-dot

9.2.13 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6/ID6	AC5/ID5	AC4/ID4	AC3/ID3	AC2/ID2	AC1/ID1	AC0/ID0

This instruction shows whether SSD1803 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be low, and then the next instruction can be performed. In this instruction you can read also the value of address counter or the part ID. When the first time the instruction is run, you can read the address counter. When the instruction is run the second time, you can read the part ID (refer to Figure 9-5).

Figure 9-5 Read Busy Flag & Address/Part ID



Part Number	Part ID
SSD1803M1V	1111111
SSD1803M2V	1111110

9.2.14 Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM. The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

9.2.15 Read Data from RAM

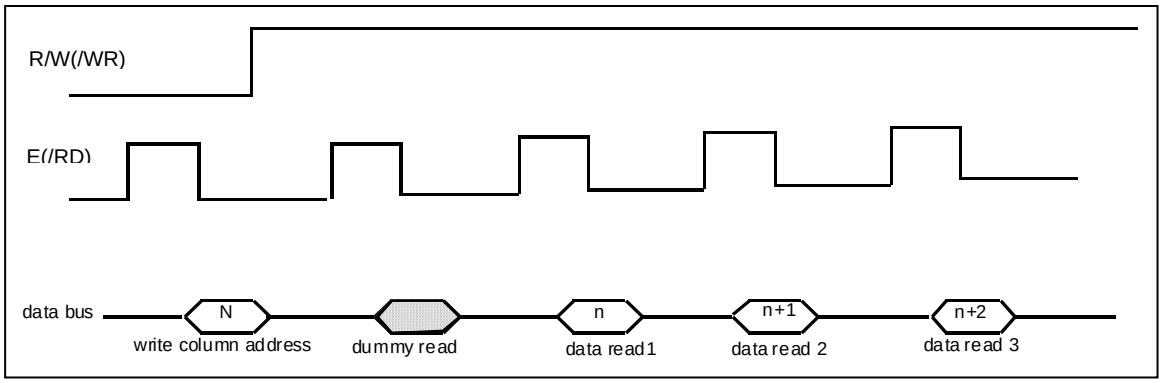
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 9-6.

Figure 9-6: Display Data Read with the insertion of dummy read



*Remark: “n” - current DDRAM address contain, “n+1” - DDRAM address+1 contain

10 INITIALIZING

10.1 Initializing by Internal Reset Circuit

When the power is turned on, SSD1803 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

Display Clear instruction
Write "20H" to all DDRAM

Set Functions instruction
DL = 1: 8-bit bus mode
N = 1: 2-line display mode
RE = 0: Extension register disable
BE = 0: CGRAM/SEGRAM blink OFF
DH = 0: Horizontal scroll enable
REV = 0: Normal display (Not reversed display)

Control Display ON/OFF instruction
D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

Set Entry Mode instruction
I/D = 1: Increment by 1
S = 0: No entire display shift
BID = 0: Normal direction segment port

Set Extension Function instruction
FW = 0: 5-dot font width character display
B/W = 0: Normal cursor (8th line)
NW = 0: Not 4-line display mode, 2-line mode is set because of N("1")

Enable Shift instruction
HS = 0000: Scroll per line disable
DS = 0000: Shift per line disable

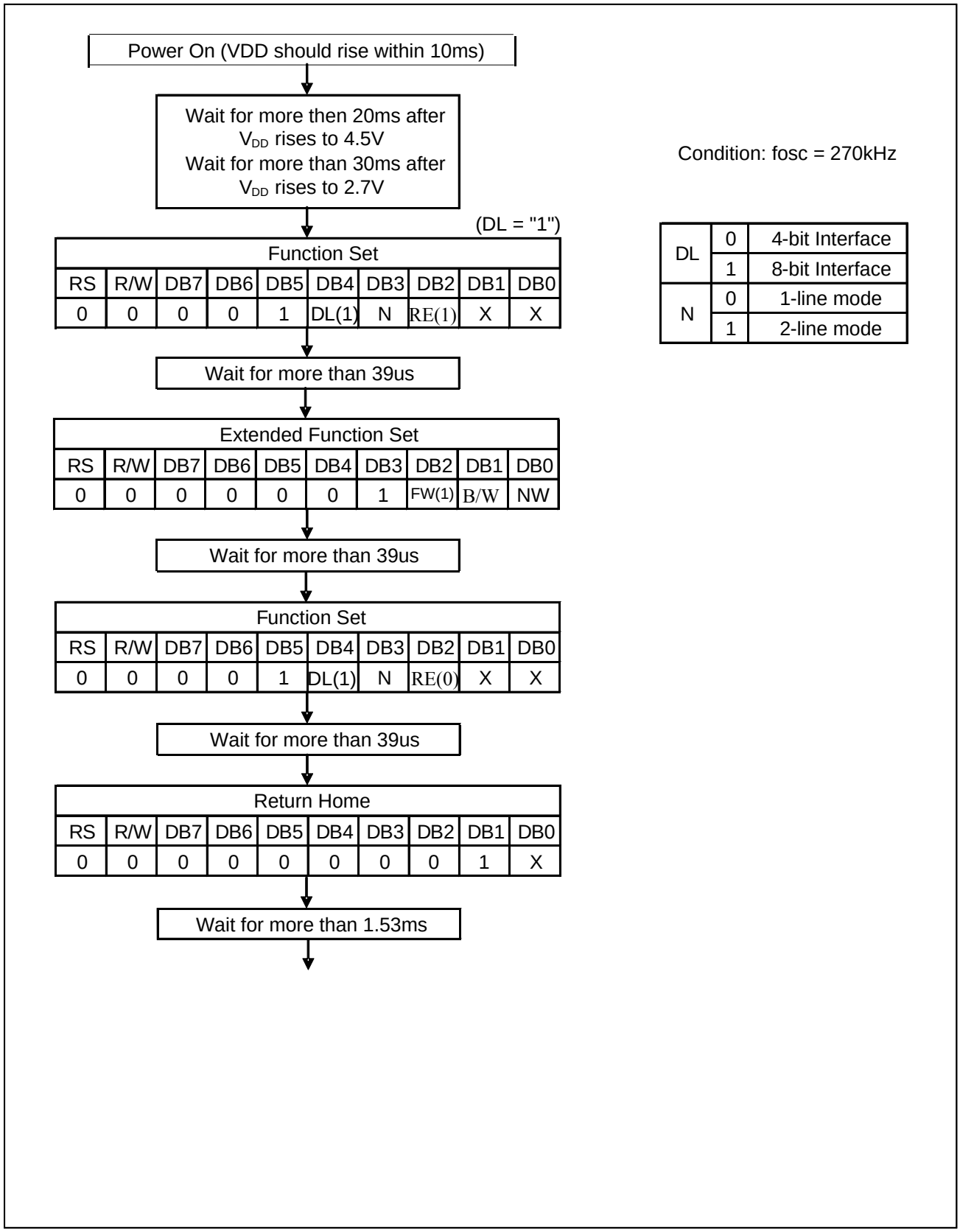
Set scroll Quantity instruction
SQ = 000000: Not scroll

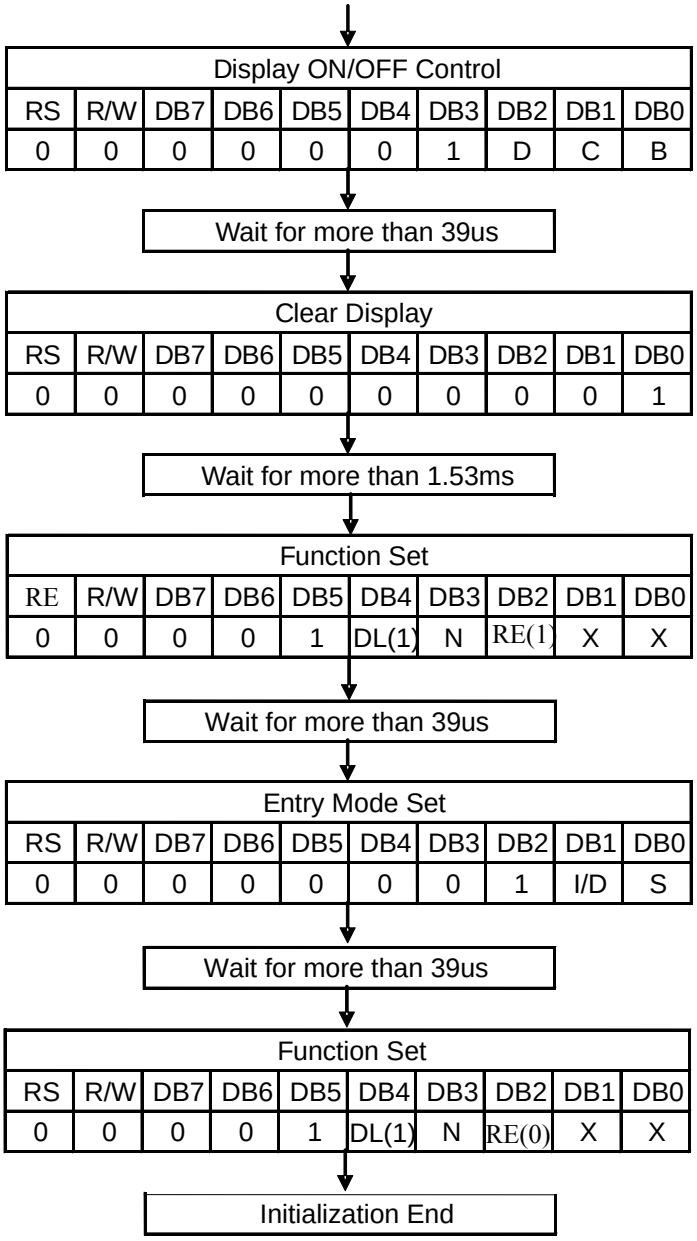
10.2 Initializing by Hardware Reset Input

When RESET pin = "Low", SSD1803 can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

10.3 Initializing by Instruction

8-BIT INTERFACE MODE

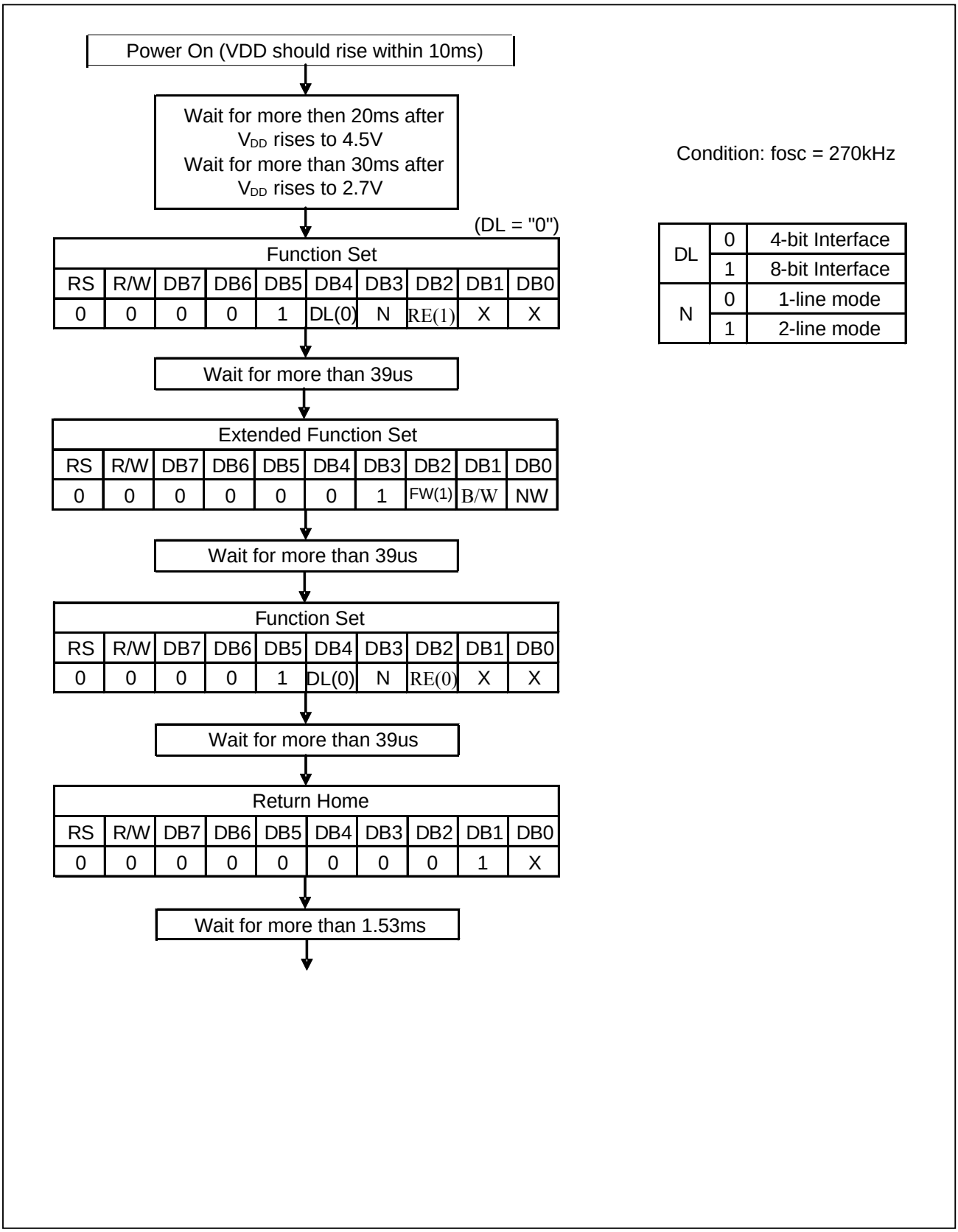


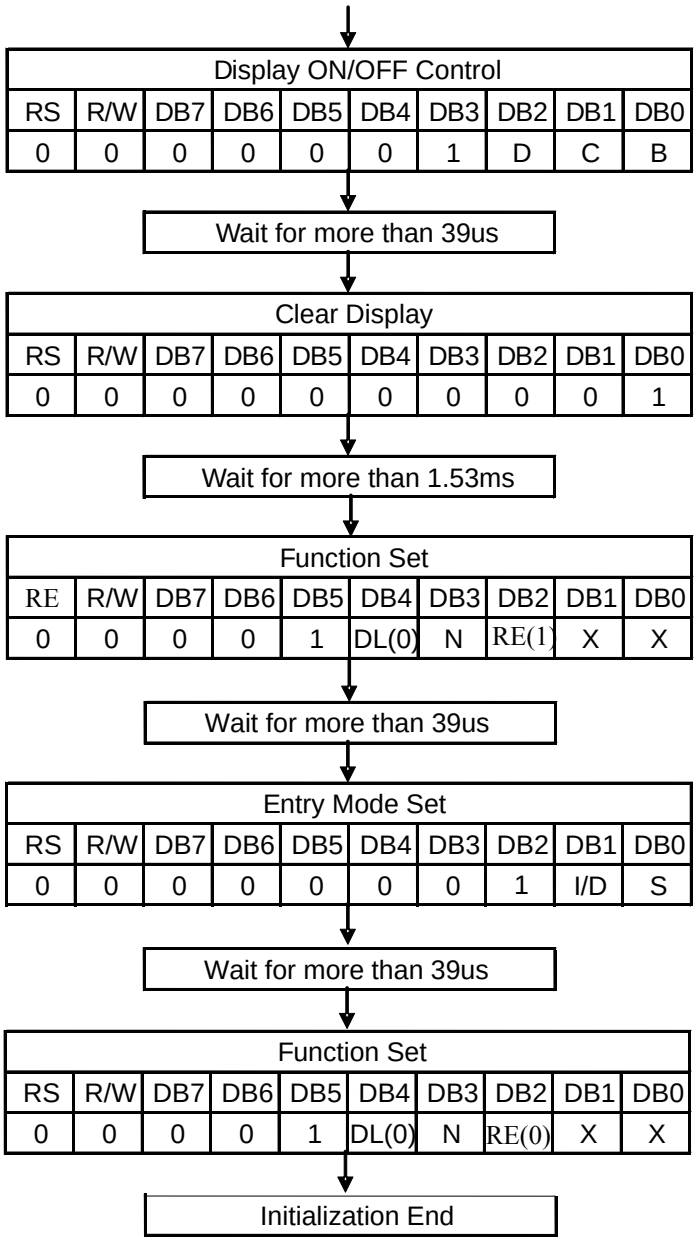


D	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
B	0	Blink off
	1	Blink on

I/D	0	Decrement Mode
	1	Increment mode
S	0	Entire shift off
	1	Entire shift on

4-BIT INTERFACE MODE



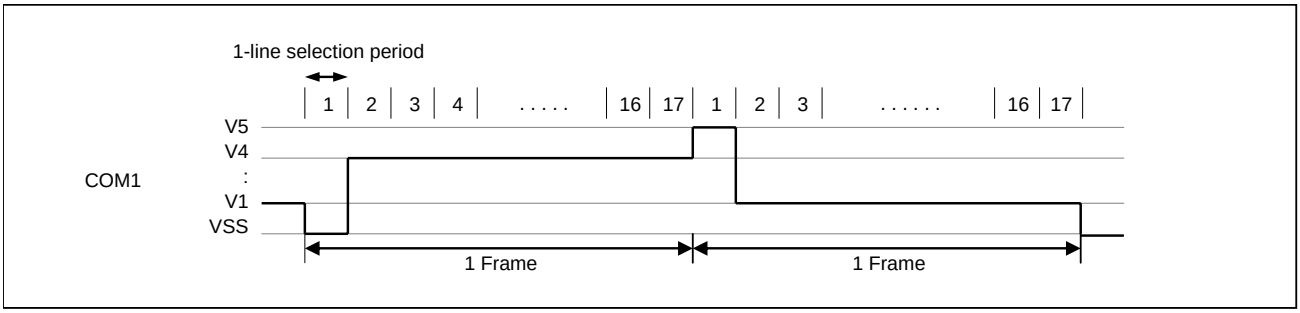


D	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
B	0	Blink off
	1	Blink on

I/D	0	Decrement Mode
	1	Increment mode
S	0	Entire shift off
	1	Entire shift on

11 FRAME FREQUENCY

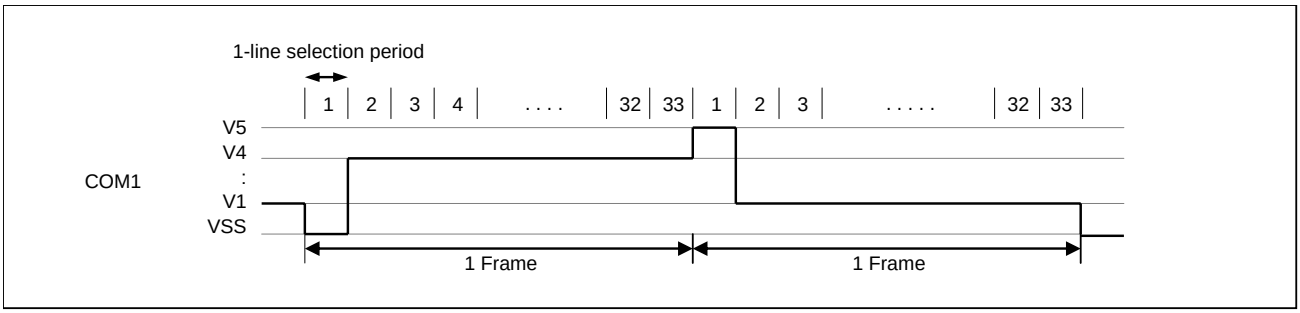
1/17 Duty Cycle



Item	Display Font Width	
	5-Dot Font Width	6-Dot Font Width
1-line selection period	200 clocks	240 clocks
Frame frequency	79.4Hz	66.2Hz

fosc = 270kHz (1 clock = 3.7us)

1/33 Duty Cycle

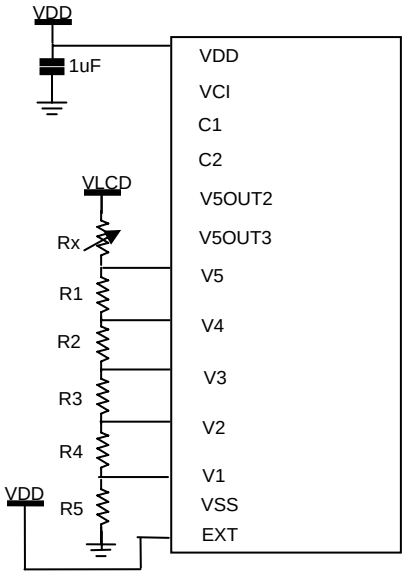


Item	Display Font Width	
	5-Dot Font Width	6-Dot Font Width
1-line selection period	100 clocks	120 clocks
Frame frequency	81.8Hz	68.2Hz

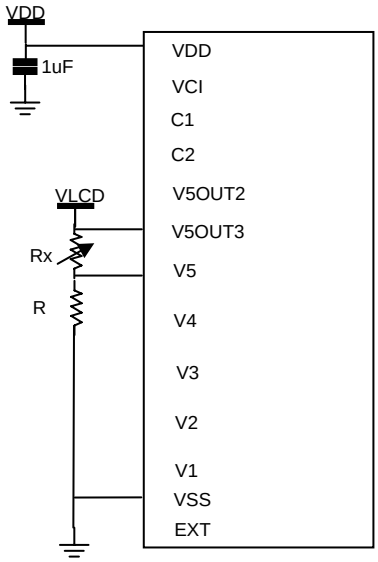
fosc = 270kHz (1 clock = 3.7us)

12 POWER SUPPLY FOR DRIVING LCD PANEL

When an External Power Supply is used



External Divider Option



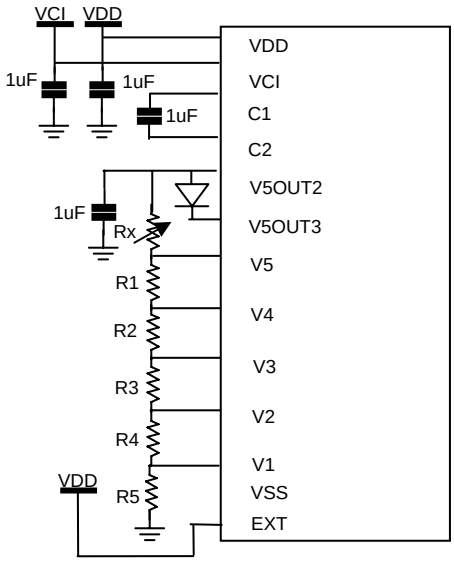
Internal Divider Option

External
Rx:47K
R1, R2, R3, R4, R5: 20K
VLCD: 13V (max)
*** Recommanded values for 1/5 bias application**

Internal
Rx: 47K
R: 100K
VLCD: 13V (max)
*** Recommanded values for 1/5 bias application**

When an Internal Booster is used

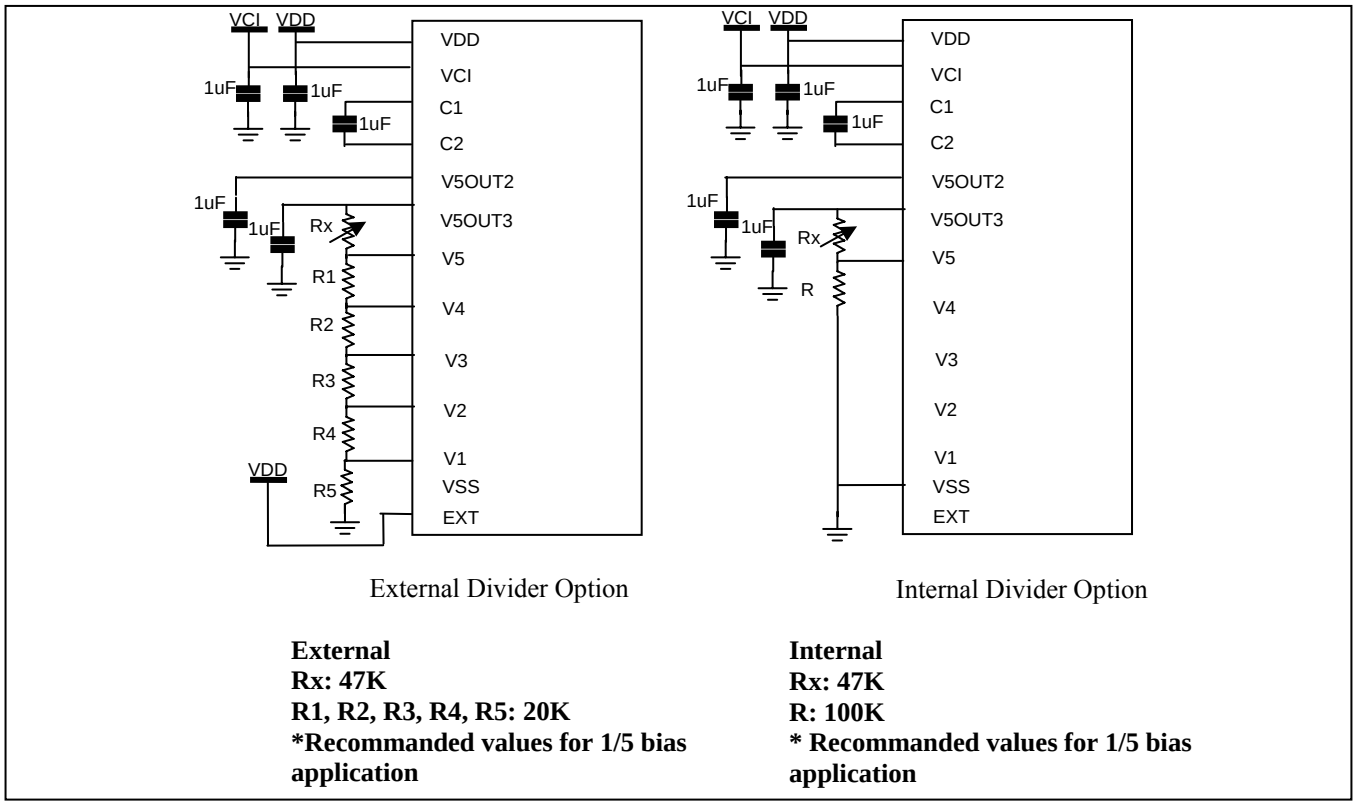
(a) Internal 2X booster



External Divider Option

External
Rx: 47K
R1, R2, R3, R4, R5: 20K
*** Recommanded values for 1/5 bias application**

(b) Internal 3X booster



Note:

- Boosted output voltage should not exceed the maximum value (13V) of the LCD driving voltage.
- The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (refer to Table 11-1)

Table 12-1 Duty Ratio and Power Supply for LCD Driving

Item	Data	
Number of lines	1	2 or 4
Duty ratio	1/17	1/33
Bias	1/5	1/6.7

13 MAXIMUM RATINGS

Table 13-1 Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage	2.7 to 3.45	V
V_{LCD}		10.0(Internal Power Supply Mode) 13.0 (External Power Supply Mode)	V
V_{IN}	Input Voltage	-0.3 to V_{DD} + 0.3	V
T_A	Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-55 to 125	°C

Voltage greater than above may damage to the circuit (V5 ≥ V4 ≥ V3≥ V2 ≥ V1≥ VSS)

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

14 DC CHARACTERISTICS

Table 14-1 DC Characteristics

(V_{DD} = 2.7 to 3.45V, Ta= -40 to 85 °C)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DD}	Operating Voltage	-		2.7	-	3.45	V
I_{DD}	Supply Current	Internal oscillation or external clock. (V_{DD} = 3.0V, f_{OSC} = 270kHz)		-	0.15	0.3	mA
V_{IH1}	Input Voltage 1 (except OSC1)	-		$0.7V_{DD}$	-	V_{DD}	V
V_{IL1}		-		-0.3	-	$0.2V_{DD}$	
V_{IH2}	Input Voltage 2 (OSC1)	-		$0.7V_{DD}$		V_{DD}	V
V_{IL2}		-		-	-	$0.2V_{DD}$	
V_{OH1}	Output Voltage 1 (DB0-DB7)	I_{OH} = -0.1mA		$0.75V_{DD}$	-	-	V
V_{OL1}		I_{OL} = 0.1mA		-	-	$0.2V_{DD}$	V
V_{OH2}	Output Voltage 2 (except DB0-DB7)	I_O = -40µA		$0.8V_{DD}$	-	-	V
V_{OL2}		I_O = 40µA		-	-	$0.2V_{DD}$	V
Vd_{COM}	Voltage Drop	I_O = ± 0.1mA		-	-	1	V
Vd_{SEG}				-	-	1	
I_{LKG}	Input Leakage Current	V_{IN} = 0V - V_{DD}		-1	-	1	µA
I_{IL}	Low Input Current	V_{IN} = 0V, V_{DD} = 3V (pull up)		-10	-50	-120	
f_{OSC}	Internal Clock (external Rf)	Rf = 75kΩ ± 2% (V_{DD} = 3.0V)		240	270	300	kHz
f_{EC}	External Clock	-		125	270	410	kHz
duty				45	50	55	%
tr, tf				-	-	0.2	µs
V_{OUT2}	Voltage Converter Out2 (Vci=3.45V)	Ta = 25 °C, C = 1µF, I_{out} = 0.25mA, f_{osc} = 270kHz		5.8	6.5	-	V
V_{OUT3}	Voltage Converter Out3 (Vci=2.7V)			7.0	7.8	-	V
VCI	Voltage Converter Input	-		2.4	-	VDD	V
V_{LCD}	LCD Driving Voltage	V5 - V_{SS}	1/4 - 1/7 bias	3.0	-	10.0	V
			External power supply mode	3.0	-	13.0	V

15 AC CHARACTERISTICS

Table 15-1 AC Characteristics

(V_{DD} = 2.7 to 3.45V, Ta= -40 to 85 °C)

Mode	Symbol	Parameter	Min	Typ	Max	Unit
(1) Write Mode (refer to Figure 15-1)	t_c	E cycle time	500	-	-	ns
	t_r, t_f	E rise/fall time	-	-	20	
	t_w	E pulse width (high, low)	230	-	-	
	t_{su1}	R/W and RS setup time	40	-	-	
	t_{h1}	R/W and RS hold time	10	-	-	
	t_{su2}	Data setup time	60	-	-	
	t_{h2}	Data hold time	10	-	-	
(2) Read Mode (refer to Figure 15-2)	t_c	E cycle time	500	-	-	ns
	t_r, t_f	E rise/fall time	-	-	20	
	t_w	E pulse width (high, low)	230	-	-	
	t_{su}	R/W and RS setup time	40	-	-	
	t_h	R/W and RS hold time	10	-	-	
	t_D	Data output delay time	-	-	160	
	t_{DH}	Data hold time	5	-	-	
(3) Serial Interface Mode (refer to Figure 15-3)	t_c	Serial clock cycle time	0.5	-	20	µs
	t_r, t_f	Serial clock rise/fall time	-	-	50	ns
	t_w	Serial clock width (high, low)	200	-	-	
	t_{su1}	Chip select setup time	60	-	-	
	t_{h1}	Chip select hold time	20	-	-	
	t_{su2}	Serial input data setup time	100	-	-	
	t_{h2}	Serial input data hold time	100	-	-	
	t_D	Serial output data delay time	-	-	160	
	t_{DH}	Serial output data hold time	5	-	-	
(4) Write Mode (refer to Figure 15-1)	t_c	E cycle time	1000	-	-	ns
	t_r, t_f	E rise/fall time	-	-	25	
	t_w	E pulse width (high, low)	450	-	-	
	t_{su1}	R/W and RS setup time	60	-	-	
	t_{h1}	R/W and RS hold time	20	-	-	
	t_{su2}	Data setup time	195	-	-	
	t_{h2}	Data hold time	10	-	-	
(5) Read Mode (refer to Figure 15-2)	t_c	E cycle time	1000	-	-	ns
	t_r, t_f	E rise/fall time	-	-	25	
	t_w	E pulse width (high, low)	450	-	-	
	t_{su}	R/W and RS setup time	60	-	-	
	t_h	R/W and RS hold time	20	-	-	
	t_D	Data output delay time	-	-	360	
	t_{DH}	Data hold time	5	-	-	
6) Serial Interface Mode (refer to Figure 15-3)	t_c	Serial clock cycle time	1	-	20	µs
	t_r, t_f	Serial clock rise/fall time	-	-	50	ns
	t_w	Serial clock width (high, low)	400	-	-	
	t_{su1}	Chip select setup time	60	-	-	
	t_{h1}	Chip select hold time	20	-	-	
	t_{su2}	Serial input data setup time	200	-	-	
	t_{h2}	Serial input data hold time	200	-	-	
	t_D	Serial output data delay time	-	-	360	
	t_{DH}	Serial output data hold time	5	-	-	

Figure 15-1 Write Mode Timing Diagram

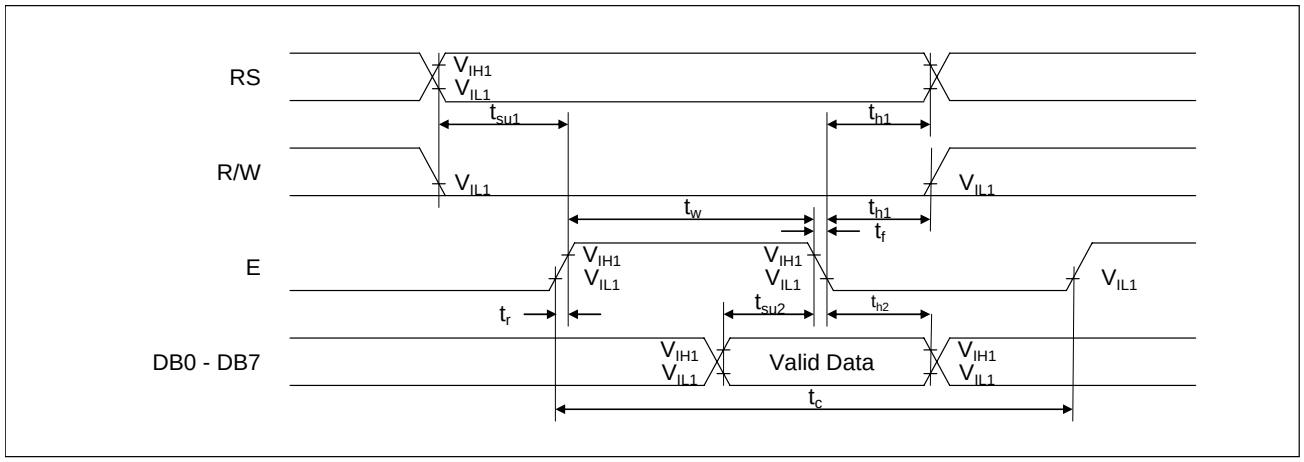


Figure 15-2 Read Mode Timing Diagram

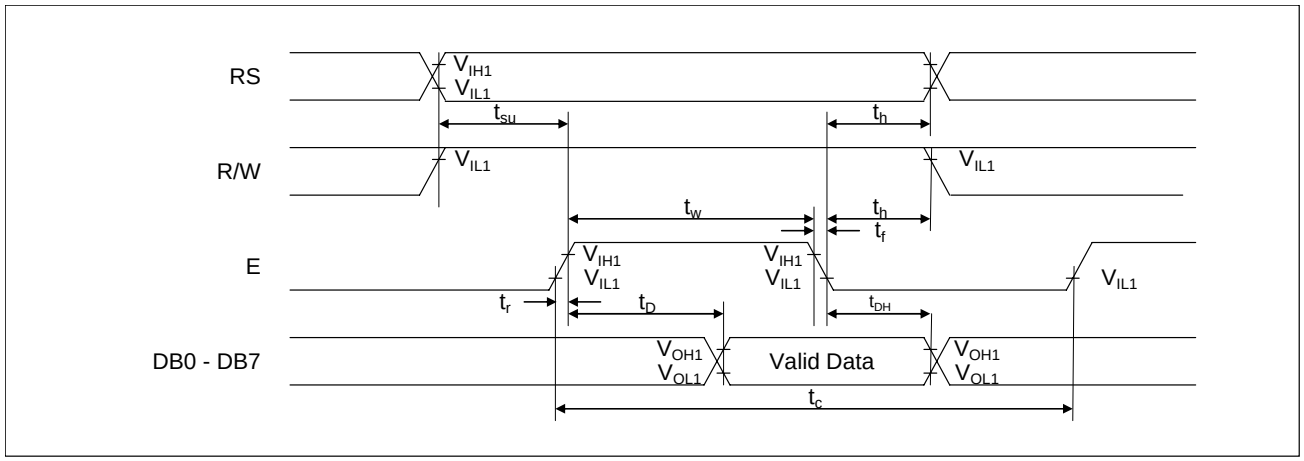


Figure 15-3 Serial Interface Mode Timing Diagram

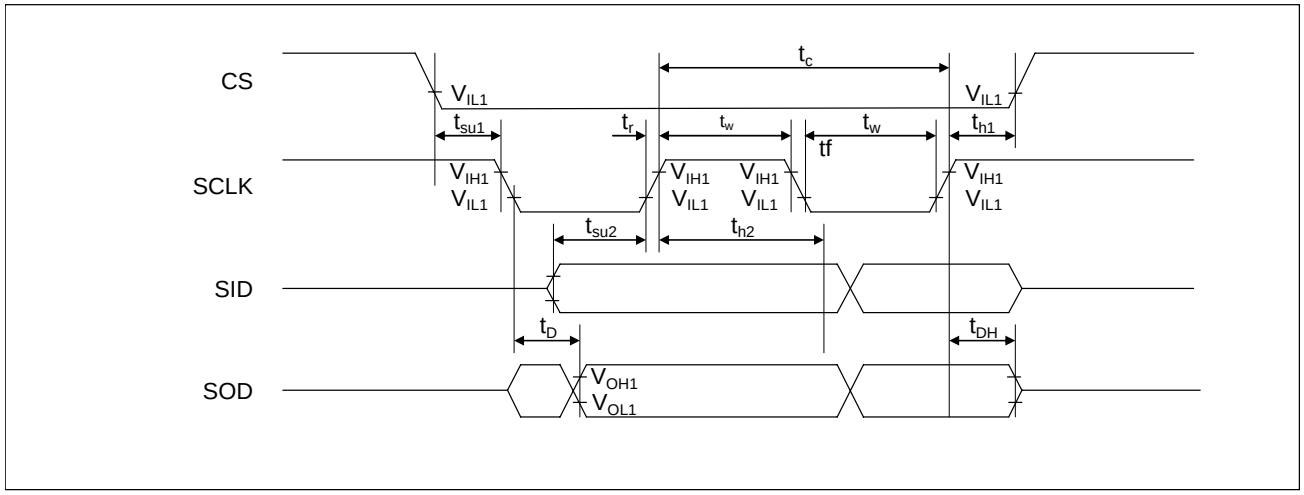
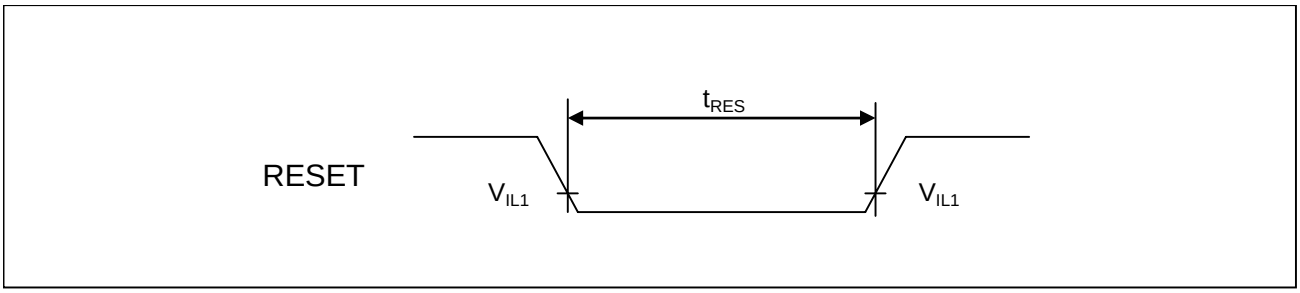


Table 15-2 Reset Timing

(V_{DD} = 2.7 to 3.45V, Ta= -40 to 85 °C)

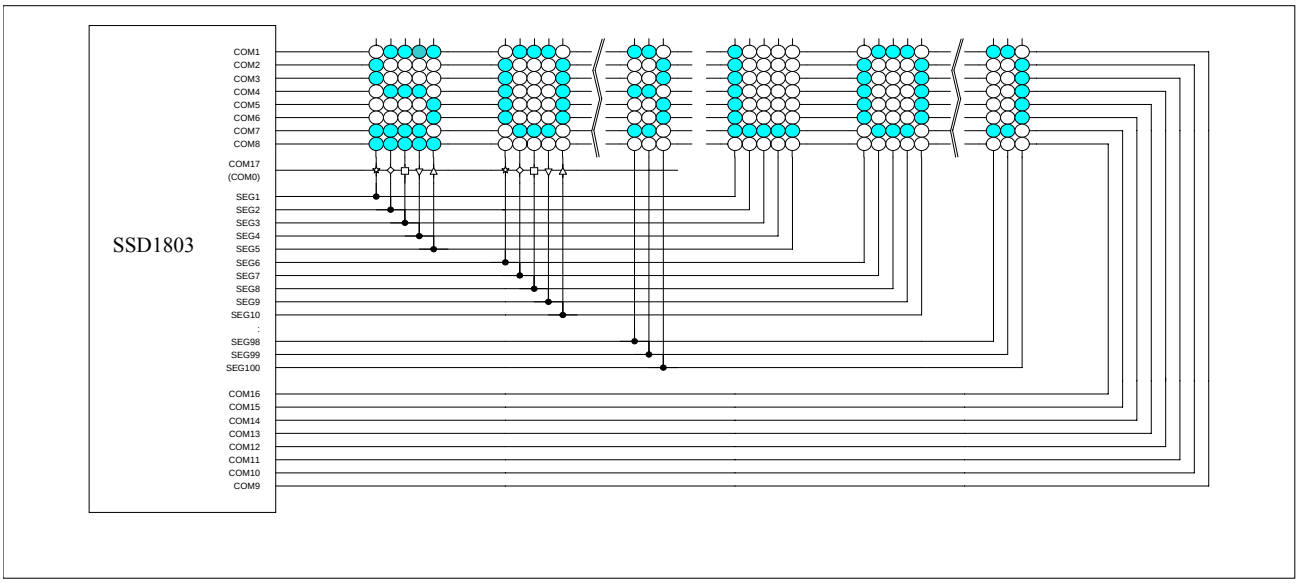
Item	Symbol	Min	Typ	Max	Unit
Reset Low level (refer to figure 15-4)	t_{RES}	10	-	-	ms

Figure 15-4 Reset Timing Diagram

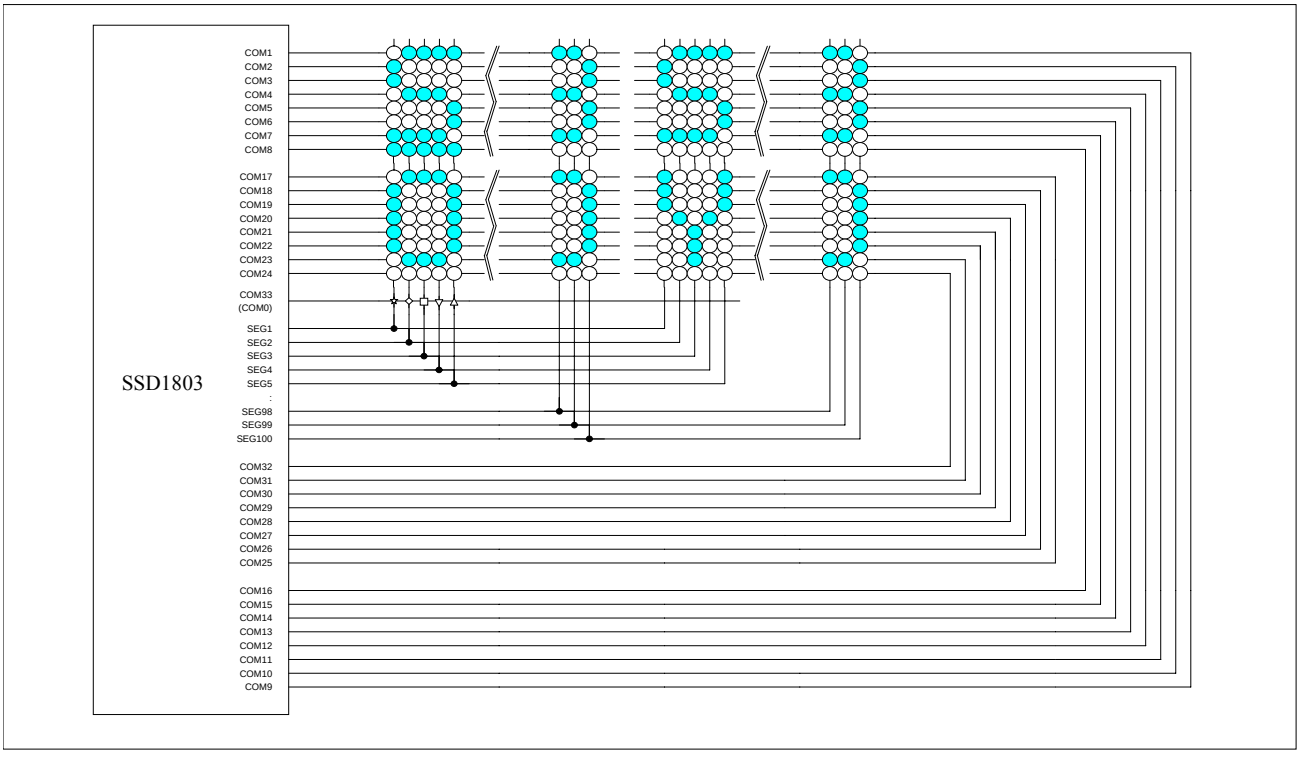


16 APPLICATION EXAMPLES

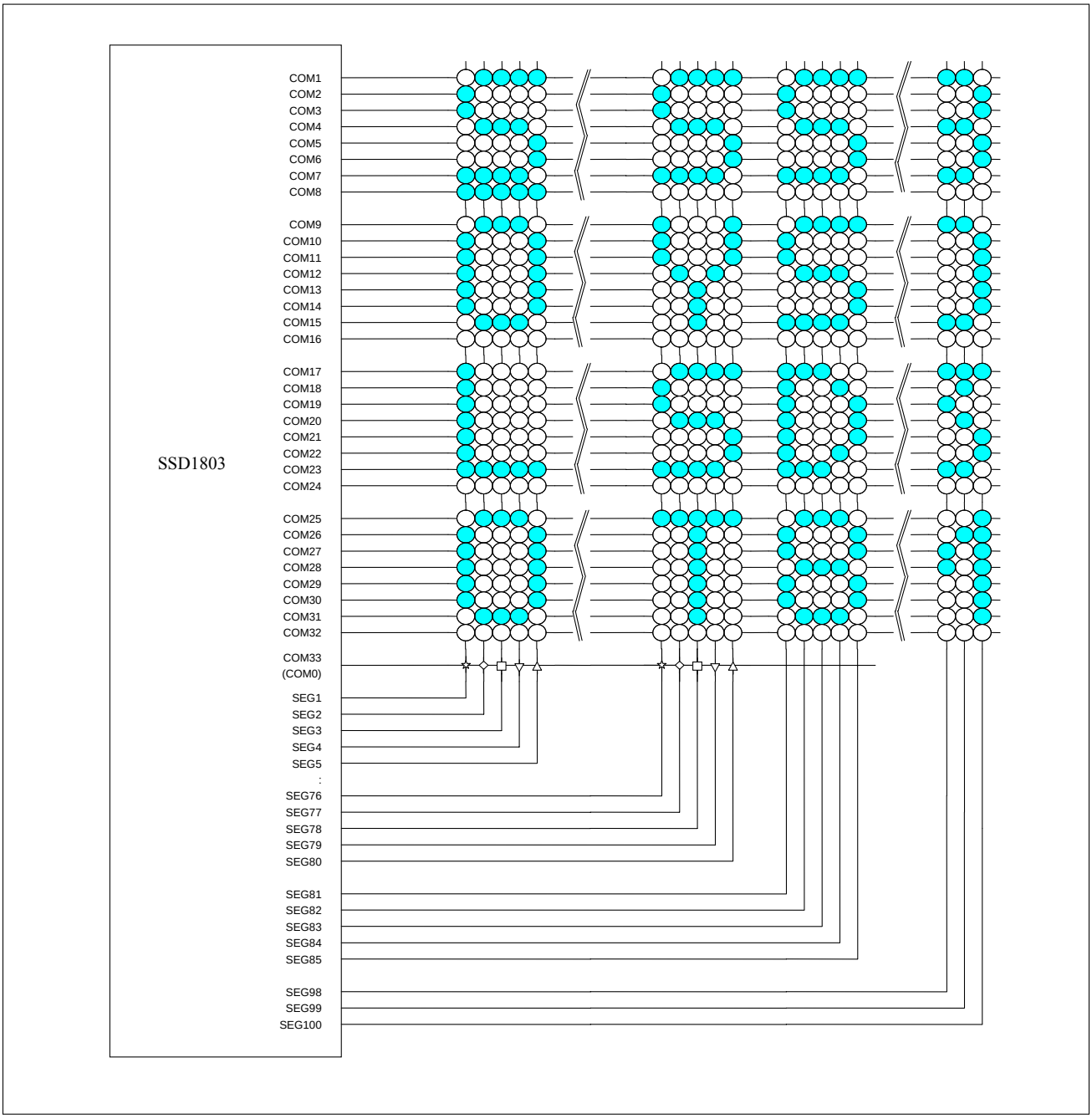
16.1 LCD Panel: 40 Character x 1-line Format (5-dot Font, 1/17 Duty)



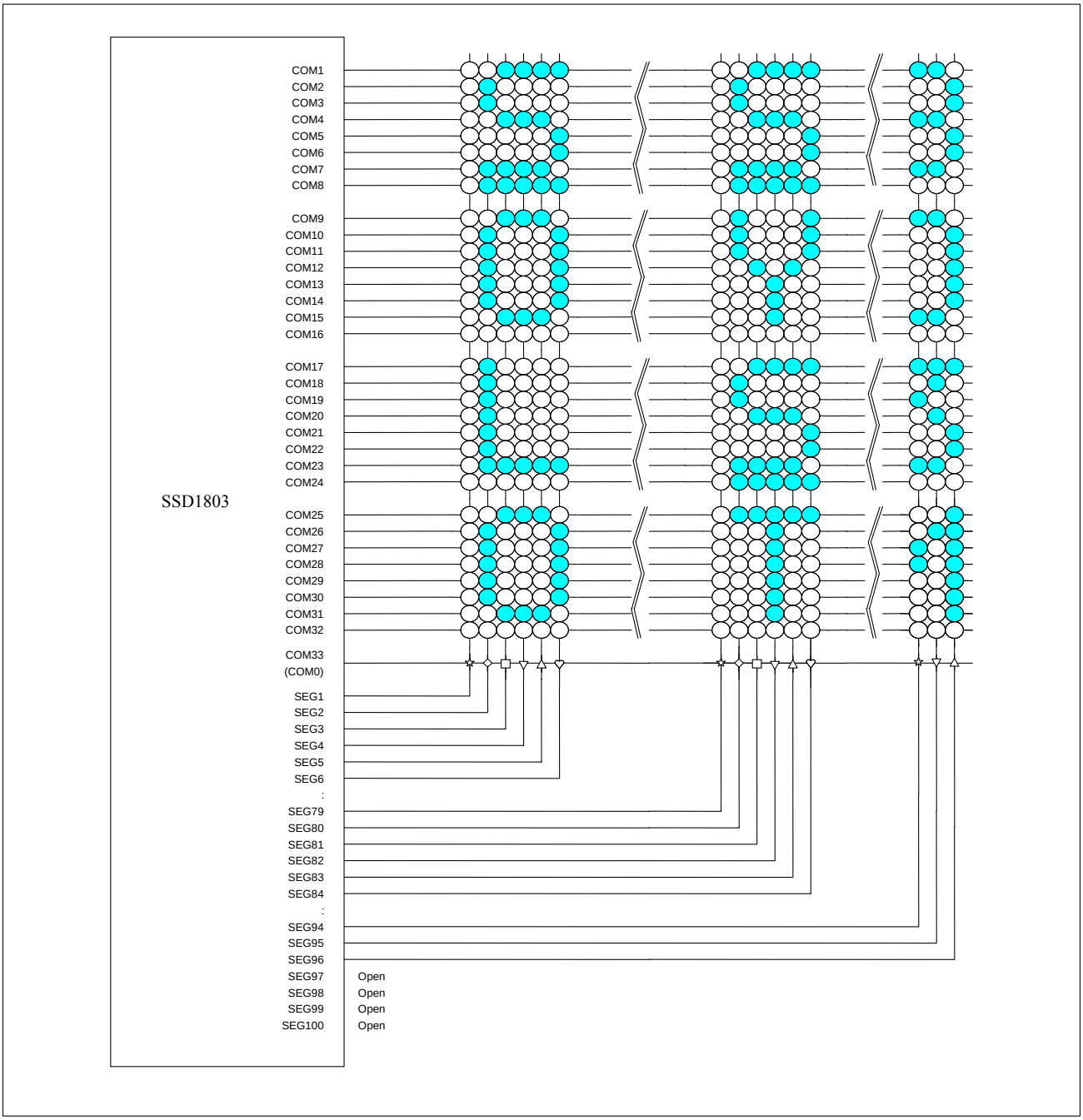
16.2 LCD Panel: 40 Character x 2-line Format (5-dot Font, 1/33 Duty)



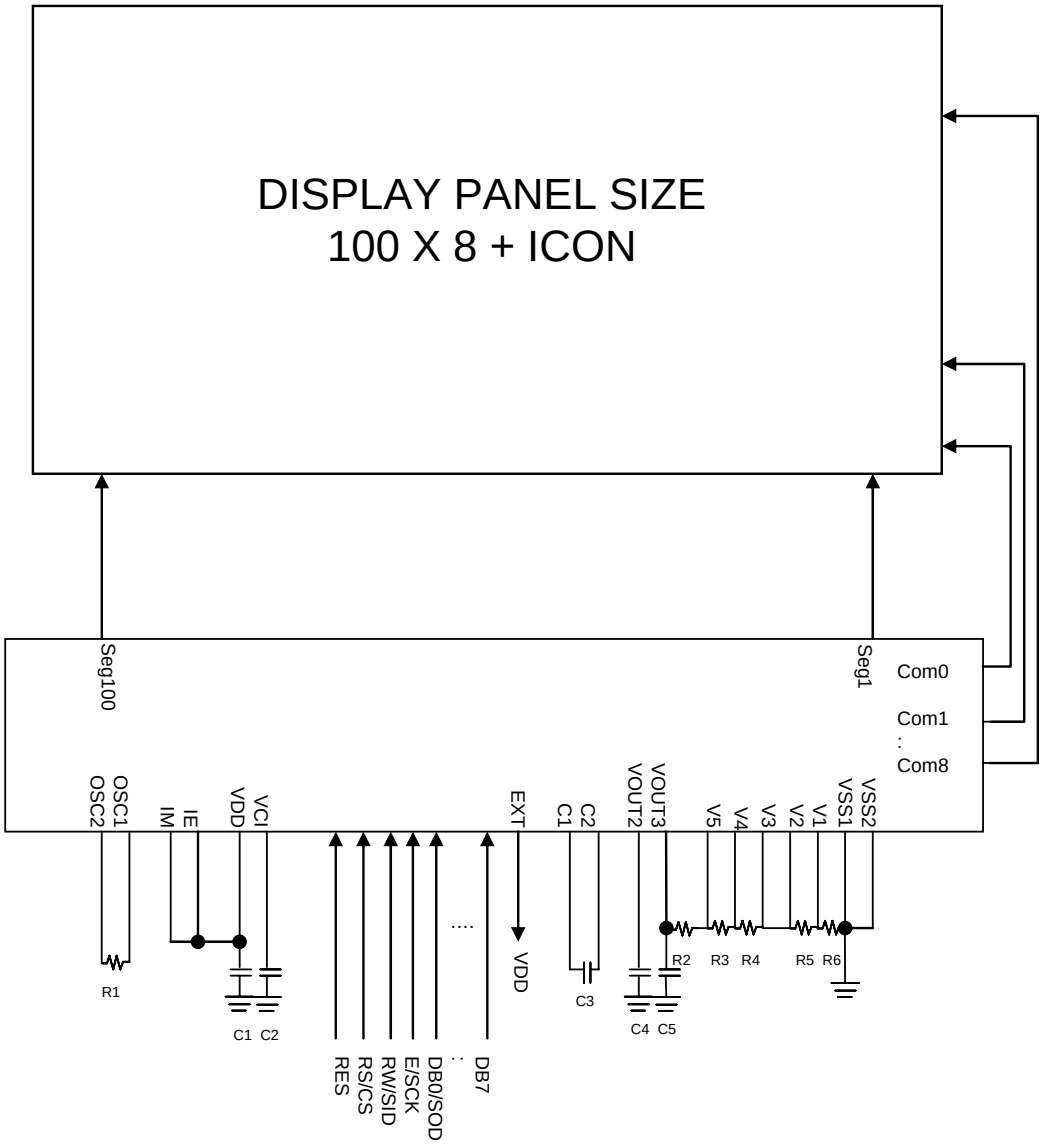
16.3 LCD Panel: 20 Character x 4-line Format (5-dot Font, 1/33 Duty)



16.4 LCD Panel: 16 Character x 4-line Format (6-dot Font, 1/33 Duty)



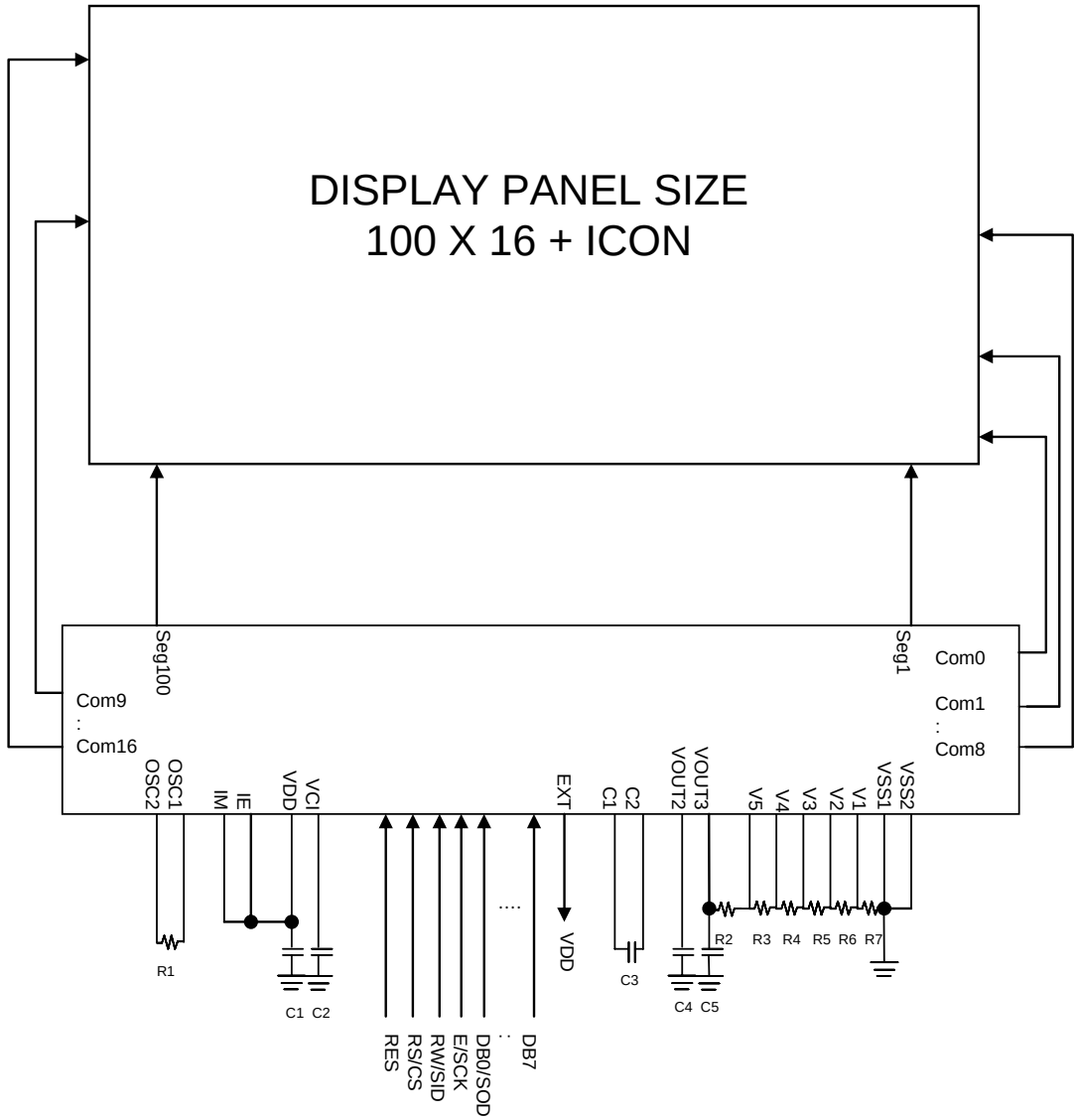
16.5 Application Circuit (1-line mode)



This is an application for 1-line, external 3X booster with external divider ¼ bias option.
Where
VCI = VDD = 3V
R1 = 75kohm
R2 = 47k ohm
R3~6 = 20kohm
C1~5 = 1uF

*Remark: The substrate of the die is connected to GND

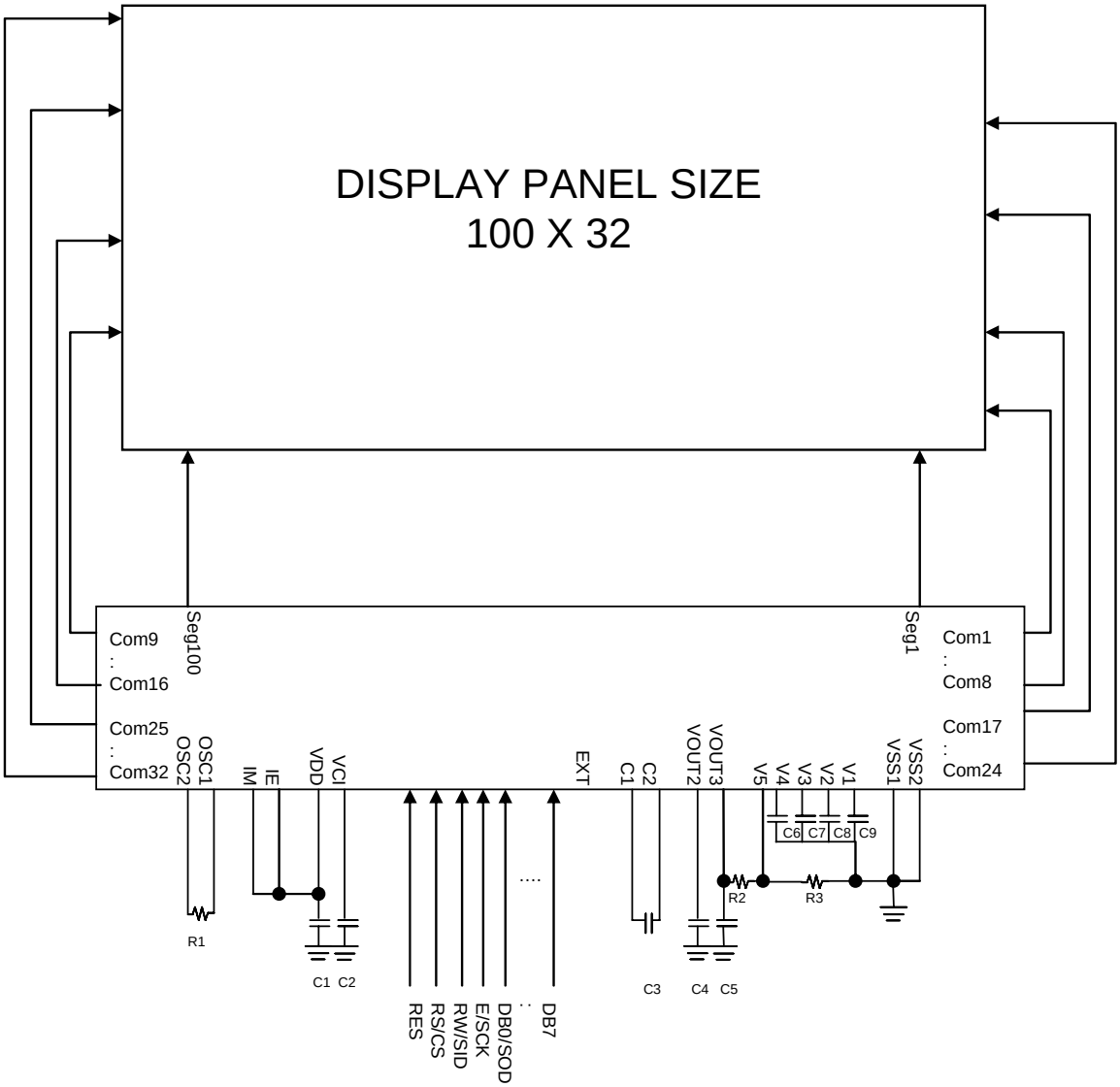
16.6 Application Circuit (2-line mode)



This is an application for 2-line, external 3X booster with external divider 1/5 bias option.
Where
VCI = VDD = 3V
R1 = 75kohm
R2 = 47k ohm
R3~7 = 20kohm
C1~5 = 1uF

*Remark: The substrate of the die is connected to GND

16.7 Application Circuit (4-line mode)



This is an application for 4-line, external 3X booster with internal divider option.
Where
VCI = VDD = 3V
R1 = 75kohm
R2 = 47kohm
R3 = 100kohm
C1~9 = 1uF

*Remark: The substrate of the die is connected to GND

17 EXAMPLE OF INSTRUCTION AND DISPLAY CORRESPONDENCE

IE = “LOW”

1. Power Supply On: Initialized by te internal power on reset circuit

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

LCD DISPLAY

2. Function Set: 8-bit, 1-line, RE(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	X	X

3. Display ON/OFF Control: Display/Cursor on

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

_

4. Entry Mode Set: Increment

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

_

5. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

S_

6. Write Data to DDRAM: Write O

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	1

SO_

7. Write Data to to DDRAM: L

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0

SOL_

8. Write Data to to DDRAM: O

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	1

SOLO_

9. Write Data to to DDRAM: M

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

LCD DISPLAY: SOLOM_

10. Write Data to to DDRAM: O

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	1

SOLOMO_

11. Write Data to to DDRAM: N

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

SOLOMON_

12. Cursor or Display Shift: Cursor shift to right

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1	X	X

SOLOMON _

13. Entry Mode Set: Entire Display Shift Enable

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

SOLOMON _

14. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

OLOMON S_

15. Write Data to DDRAM: Write Y

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	1	0	0	1

LOMON SY_

16. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

OMON SYS_

17. Write Data to DDRAM: Write T

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	1	0	0

LCD DISPLAY

MON SYST_

18. Write Data to DDRAM: Write E

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	1

ON SYSTE_

19. Write Data to DDRAM: Write C

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	1

N SYSTEC_

20. Write Data to DDRAM: Write K

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

SYSTECK_

21. Cursor or Display Shift: Cursor shift left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	X	X

SYSTECK

22. Write Data to DDRAM: Write H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	0

SYSTECH_

23. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

SOLOMON SYSTECH

24. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

_

IE = “HIGH”

1. Power Supply On: Initialized by te internal power on reset circuit

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Function Set: 8-bit, RE(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

3. Extended Function Set: 5-font, 4-line

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	1

4. Function set: RE(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

5. Display ON/OFF Control: Display/Cursor on

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

6. Write Data to DDRAM: Write S

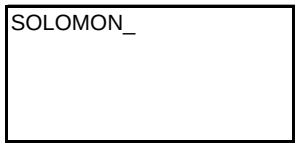
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

7. Write Data to DDRAM: Write O

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	1

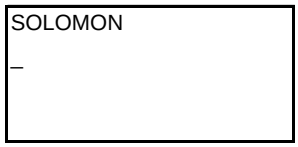
12. Write Data to DDRAM: Write N

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0



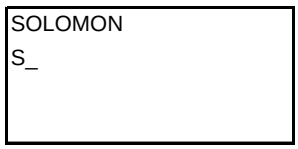
13. Set DDRAM Address 20H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0



14. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

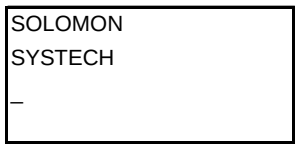


20. Write Data to DDRAM: Write H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	0

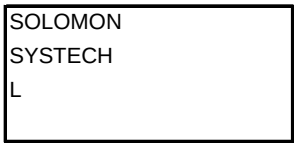
21. Set DDRAM Address 40H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0



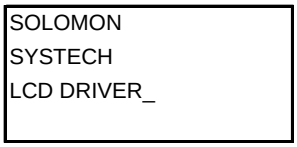
22. Write Data to DDRAM: Write L

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0



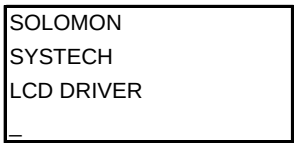
31. Write Data to DDRAM: Write R

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0



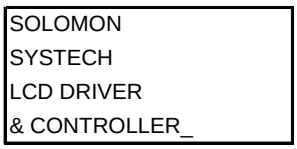
32. Set DDRAM Address 60H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0



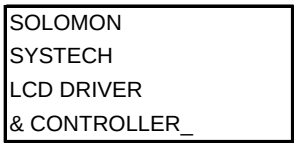
44. Write Data to DDRAM: Write R

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0



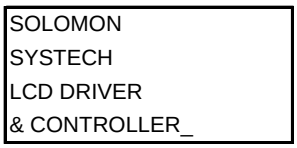
45. Function Set: RE(0), DH(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0



46. Function Set: RE(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0



47. Shift/Scroll Enable: DS4(1), DS3/2/1(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	0	0

SOLOMON
SYSTECH
LCD DRIVER
& CONTROLLER_

48. Function Set: RE(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0

SOLOMON
SYSTECH
LCD DRIVER
& CONTROLLER_

49. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SOLOMON
SYSTECH
LCD DRIVER
CONTROLLER_

50. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SOLOMON
SYSTECH
LCD DRIVER
CONTROLLER_

51. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SOLOMON
SYSTECH
LCD DRIVER
ONTROLLER_

52. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SOLOMON
SYSTECH
LCD DRIVER
NTROLLER_

53. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

54. Function Set: RE(0), REV(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	1

55. Cursor or Display Shift: Display shift to right

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

56. Cursor or Display Shift: Display shift to right

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

57. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

58. Function Set: RE(0), REV(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

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LCD DRIVER
& CONTROLLER

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59. Function Set: RE(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

60. Entry Mode Set: BID(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

61. Write Data to DDRAM: Write B

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	0

62. Write Data to DDRAM: Write I

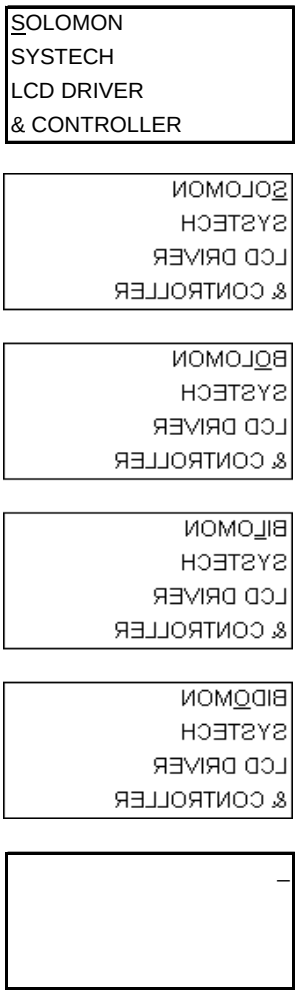
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	1

63. Write Data to DDRAM: Write D

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

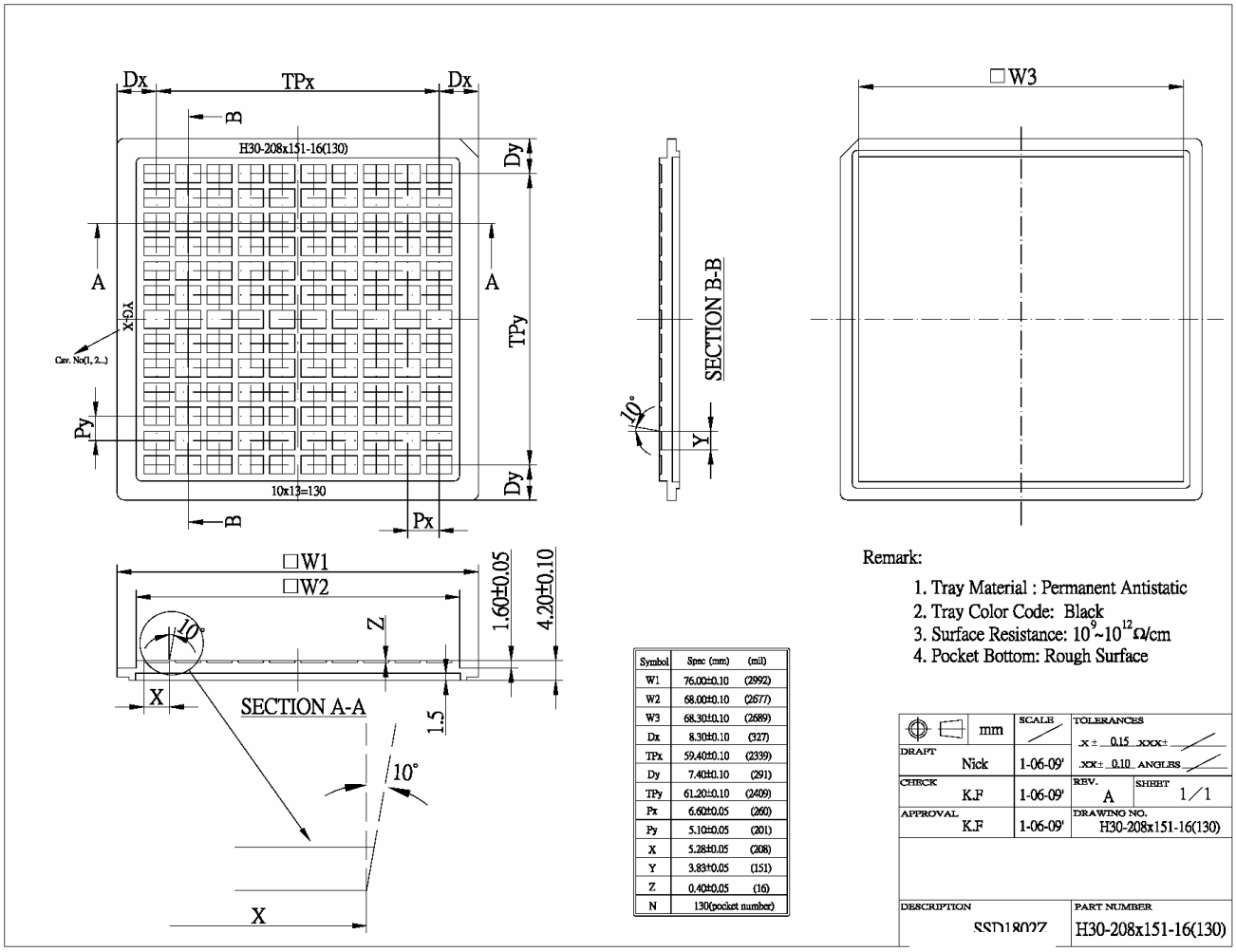
64. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1



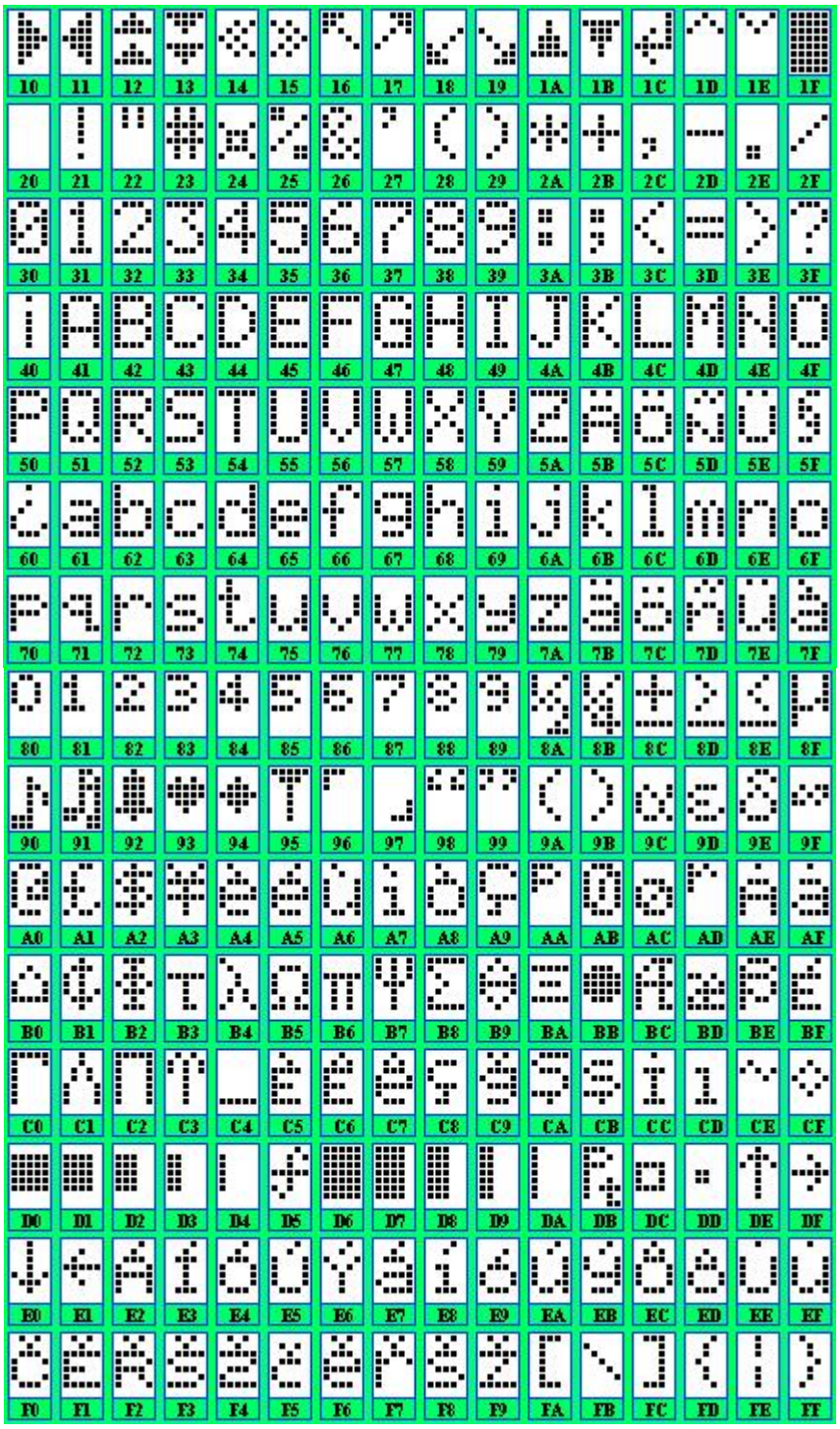
18 PACKAGE INFORMATION

18.1 DIE TRAY DIMENSIONS

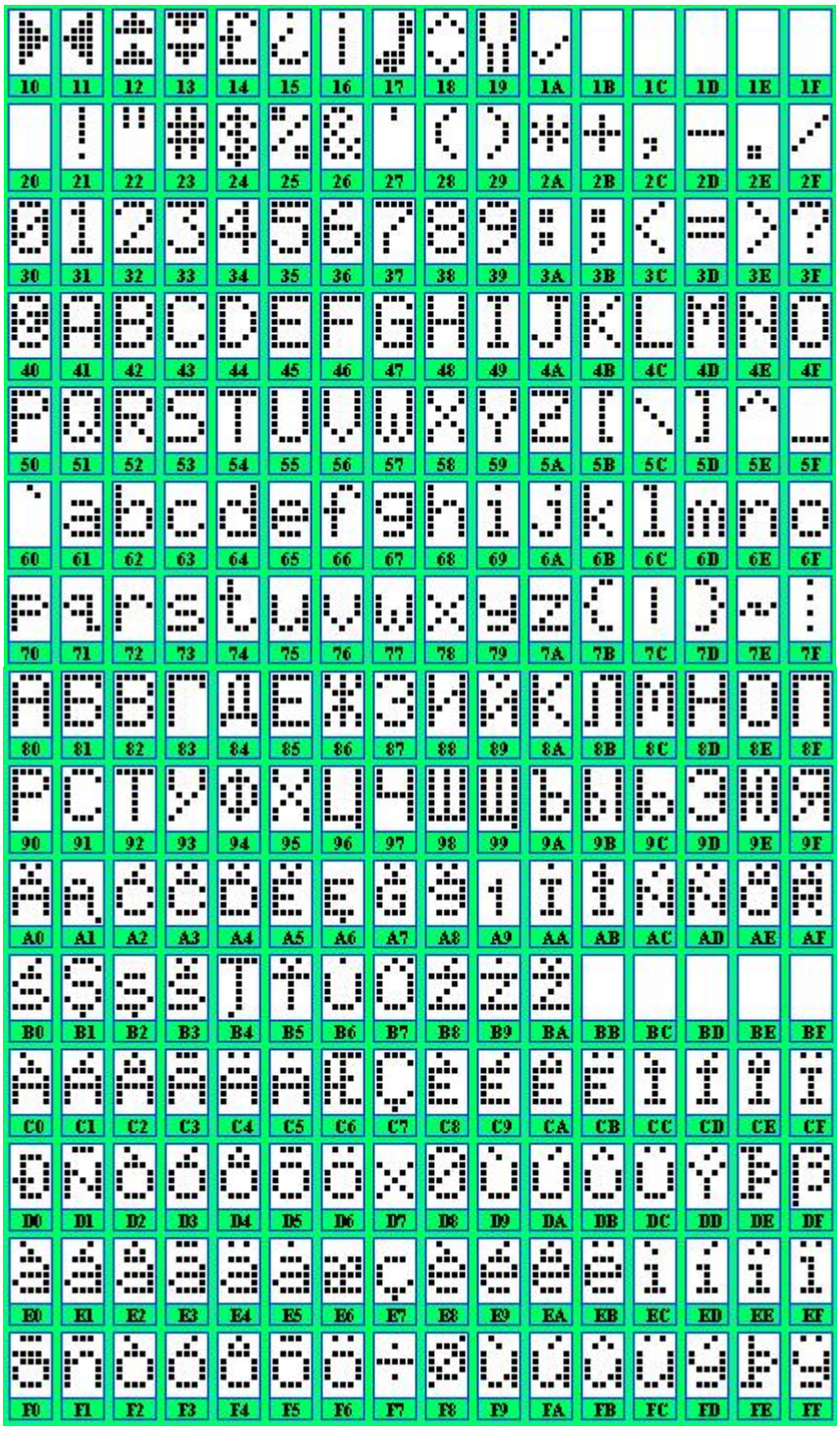


Symbol	Spec (mm)	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
Dx	8.30±0.10	(327)
TPx	59.40±0.10	(2339)
Dy	7.40±0.10	(291)
TPy	61.20±0.10	(2409)
Px	6.60±0.05	(260)
Py	5.10±0.05	(201)
X	5.28±0.05	(208)
Y	3.83±0.05	(151)
Z	0.40±0.05	(16)
N	130(pocket number)	

APPENDIX I SSD1803M1 CGROM CHARACTER CODE



APPENDIX II SSD1803M2 CGROM CHARACTER CODE



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

http://www.solomon-systech.com